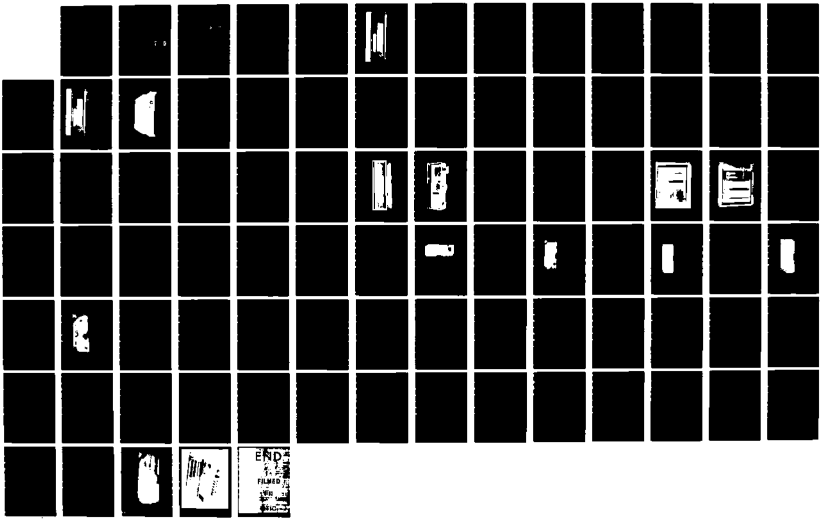
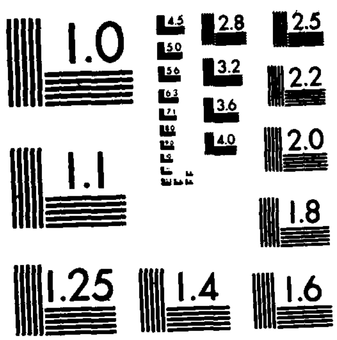
AD-A128 582   DIGITAL PROCESSING CLOCK AND REMOTE DISPLAY UNITS   1/1
TECHNICAL OPERATION AND MAINTENANCE MANUAL(U) NAVAL
RESEARCH LAB WASHINGTON DC   NOV 76 NRL-IB-166

UNCLASSIFIED   F/G 14/2   NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(1)

NRL Instruction Book 166

AD A128502

Digital Processing Clock
and
Remote Display Units
Technical Operation and Maintenance Manual

November 1976

Sponsored by Naval Sea Systems Command

NAVAL RESEARCH LABORATORY
Washington, D.C.

Approved for public release: distribution unlimited

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

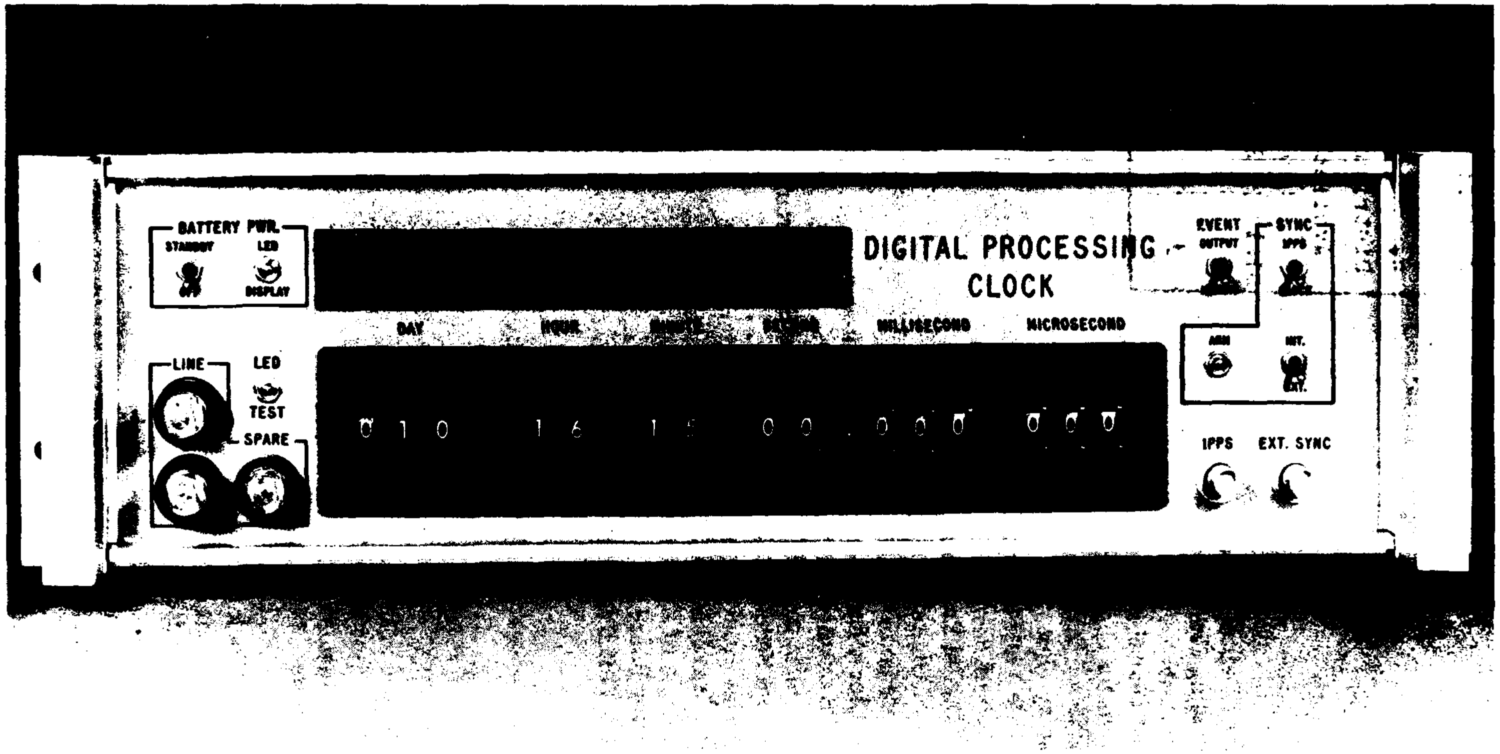


Fig. 1-0—Front View of Digital Processing Clock

I.

CHAPTER 1

GENERAL INFORMATION

1-1 Introduction

The Digital Processing Clock is designed to make precision time available in visual and electronic form. The system consists of one digital processing clock and four remote display units and contains state-of-the-art electronic devices. In all instances where it has been available, military-specified hardware has been utilized. The clock provides all necessary timing information to enable the generation of a wide range of time codes and time related information for future applications.

Figure 1-0 gives a front view of the Digital Processing Clock. The clock is human engineered for easy setting. It is designed to be driven by precision frequency standards such as cesium beams, rubidium vapor standards, disciplined time and frequency standards, or any other precision frequency standard providing an adequate 1 MHz output, but will operate on its own internal oscillator if no precision standard is available. The clock is capable of being set to an accuracy within 1 microsecond (μs) to an applied external pulse. This pulse need not occur on precise 1 second intervals; prior knowledge of when the pulse will occur is used to preset the thumbwheel switches on the front of the clock.

1-2 General Theory

In addition to the display of the precise time in days, hours, minutes and seconds, the Digital Processing Clock produces (a) a parallel time code output that is capable of driving from one to four remote display units (Figure 1-1) at distances well removed from the clock itself, (b) two separate selectable time of event (TOE) output pulses which can be used to synchronize other equipments, and (c) pulse outputs of 1 pulse per second (PPS)

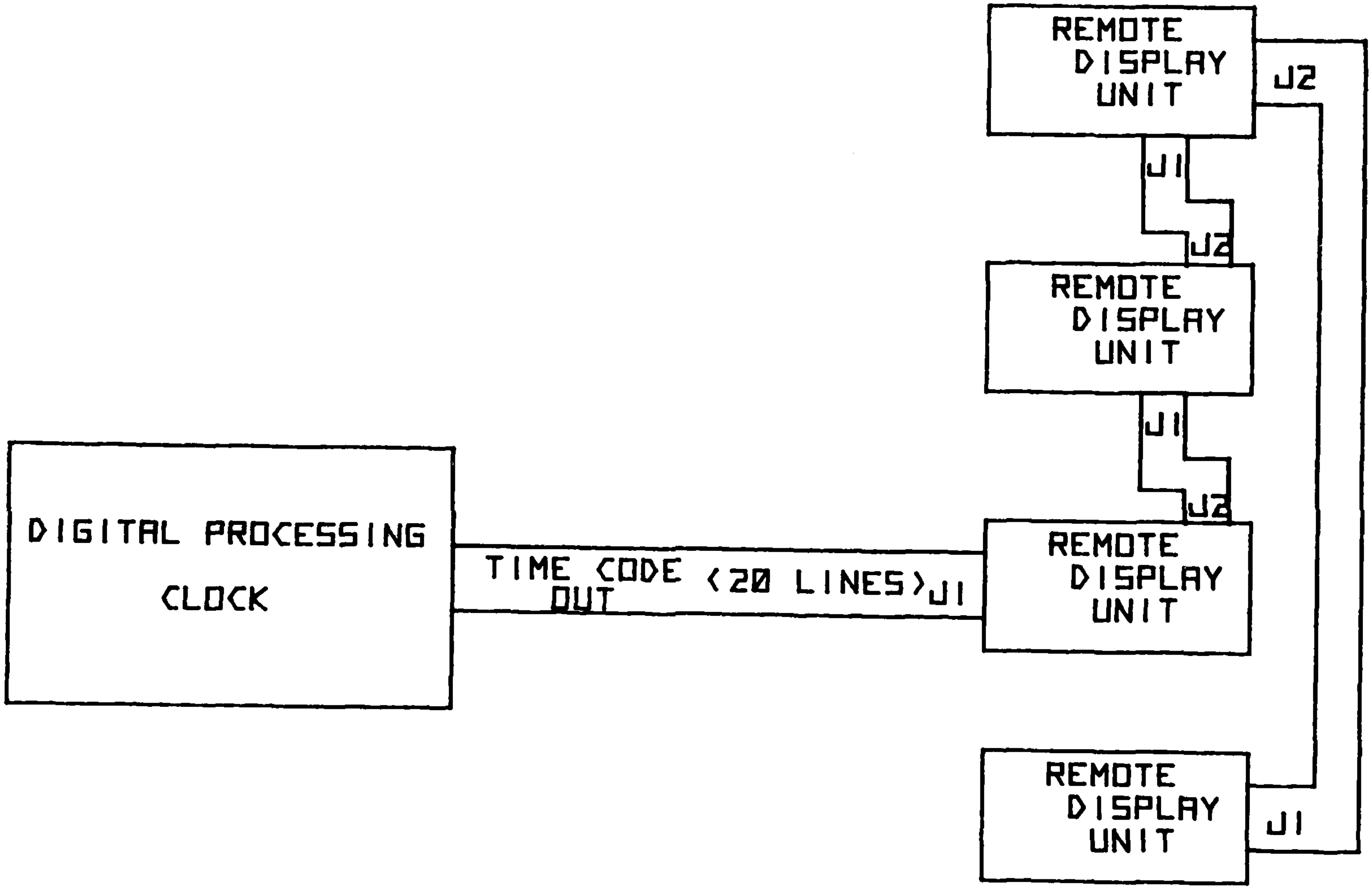


Fig. 1-1—Digital Processing Clock System

and 1 pulse per ten seconds (PP10S). Figure 1-1 shows a block diagram of the Digital Processing Clock system. Functionally, the Digital Processing Clock consists of seven sections:

(1) Power Supply (Figure 4-1)

(2) Battery Pack (Figure 4-1)

(3) Clock Time Base and Display Circuit (Figure 6-1A)

(4) 1 MHz to 1 PPS Countdown and Sync (Figure 6-2A)

(5) Day Hour Minute Second Counter (Figure 6-3A)

(6) Time of Event Circuit (Figure 6-4A)

(7) 5 Volt Regulator (Figure 6-5A)

In addition, as shown in Figure 2-1 (Operator Controls), the Digital Processing Clock contains a 15 unit decade thumbwheel switch used for time setting, delay insertion, and time of event operations. Also included are front panel switches used to select specific modes of clock operation. Built in test equipment (BITE) eases the operator's job in checking that the clock is functioning correctly. Battery backup is supplied internally to assure correct time through short power interruptions, such as ship to shore power switchover.

1-3 Performance Specification for Digital Processing Clock/Remote Display Unit

The Digital Processing Clock with remote display has a minimum the performance characteristics listed in the following subsections.

1-3-1.0 General Description

The clock (time code generator) with remote display is capable of the following functions:

(1) Generation of continuous real time in days, hours, minutes, and seconds

(2) Generation of a time tick pulse (1 PPS) which can be synchronized to within 1 μs of any externally applied pulse

(3) Generation of a time of event output pulse (TOE) which can be externally programmed to occur at any desired time

(4) Capability of being driven either by an external standard or of operating from its own internal oscillator. Means have been provided to ensure continuous reading of time in the absence of an external reference signal.

(5) Capable of driving four remote display units

(6) Readout ability to receive the time code produced by the clock/time generator and drive a display that indicates the continuously updated time of day from the clock

1-3-2.0 Mechanical and Electrical Requirements

1-3-2.1 Enclosure

The equipment is contained in a single dustproof unit capable of rack mounting in an Electronic Industry Association (EIA) Standard 48.3 cm (19-in.) rack with universal hole spacing. Slides will be optional. The remote readout is contained in a single, separate, dustproof unit capable of rack mounting. The unit shall occupy no more than 14.0 cm (5½ in) of vertical rack space and shall be no greater than 55.9 cm (22 in) deep.

1-3-2.2 Modularity

Except for the power supply and battery, the equipment is of modular construction using plug-in repairable circuit boards designed on a function basis to the maximum extent possible.

1-3-2.3 Size

The equipment has maximum dimensions of 48.3 cm (19 in) width, 14.0 cm (5½ in) vertical rack space and 55.9 cm (22 in) depth. The remote display has maximum dimensions of 35.6 cm (14 in) width, 8.9 cm (3½ in) vertical rack space, and 12.7 cm (5 in) depth excluding connectors.

1-3-2.4 Power

The unit contains its own regulated power supply. This supply operates off single phase, alternating current supplied at: 115V (±10%) and 60 HZ (± 3%.)

1-3-2.5 Fuses

Fuses have been provided as required to protect circuits from power surges.

1-3-2.6 Cooling

A means for minimizing temperature within the equipment box is required. Heat sinks or equivalent similar means to lower equipment ambient have been used and are located at the rear of the unit. Blowers or fans have not been used.

1-3-2.7 Battery

Sealed gel-cell batteries provide continuous operation for 1/2 hr. in case of power failure.

1-3-3.0 Functional Description

1-3-3.1 Clock/Time Code Generator

All outputs are through BNC connectors unless otherwise specified. The outputs are as follows:

1-3-3.1.1 Time of Day

The time of day information is sent out on 20 binary-coded decimal (BCD) parallel lines using a Cannon SK-24-31SL connector.

1-3-3.1.2 Tick (1PPS) Output

The 1 PPS output is a 20 μs long pulse which recurs each second and is capable of being set to within 1 μs of any externally applied synchronizing pulse. This pulse is also capable of being advanced or retarded in 1 μs steps through the use of decade thumbwheel switches on the front panel. The output impedance is 50 Ω.

1-3-3-1.3 Tick (1PP10S) Output

A 1 PP10S output is available with an output impedance of 50 Ω.

1-3-3-1.4 Time of Event Output

The TOE output is a 20 μs pulse which occurs at a preset time programmed into the clock with decade thumbwheel switches.

1-3-3-1.5 Time Interval Output

The rate at which this Time of Event pulse recurs can be selected by dual in-line package (DIP) rocker switches on Time of Event Circuit Board as follows: once/sec, once/10 sec, once/minute, once/hour, and once/day. It may also be inhibited so that it does not occur at all.

1-3-3.2 Remote Display

The remote display unit is capable of translating the time of day information d :'bed in 1-3-3.1.1 and displaying it on a continuously updated time of day display.

1-3-3.2.1 Input Impedance

The input impedance is the equivalent of one regular transistor-transistor-logic (_ _) gate.

1-3-3.2.2 Input Levels

The inputs levels are TTL compatible.

1-3-3.3 Operator Controls

All operator controls for setting the time, synchronization, switching of functions, etc., are on the front panel of the unit or are easily accessible when the unit is installed in its equipment rack.

1-3-3.3.1 Indicator Lamps

Indicator lights are provided to show when the Arm/Ready condition exists. A coincidence indicator between the synchronization input and the 1PPS output of the clock is provided.

1-3-3.3.2 Time Display

Generated time in decimal format in days, hours, minutes, and seconds is displayed on a planer readout. The display is clearly visible and readable at a distance of 2.74 m (9 feet) and in the horizontal plane at angles of plus or minus 60 degrees. A minimum height of 0.64 cm (0.25 in) for the display characters is used.

1-3-4.0 Testing

The equipment was designed for testing in accordance with MIL-E-16400 for shock, vibration, temperature, humidity, and EMC but has not been subjected to the full range of tests. The unit has been demonstrated to meet all operating performance criteria including, but not limited to, time base accuracy and stability for the following tests:

1. Temperature in accordance with Class IV of MIL-E-16400F (0°C to 50°C). Clock was additionally tested to −25°C successfully
2. Vibration in accordance with MIL-E-16400F in three different planes; 5 min at each cycle, 5 to 30 Hz, in each plane; 2 hrs. at 33 Hz in each plane;
3. Shock in accordance with MIL-E-16400F in three different planes: 181.4 kg (400 lb.) hammer blows from 30.5 cm (1 ft.), 91.4 cm (3 ft.) and 152.4 cm (5 ft.) levels.

CHAPTER 2

OPERATION

The Digital Processing Clock is human engineered for easy operation. Figure 2-1 shows Operator Controls and Built-In-Test Equipment (BITE) indicators on the front panel. Figures 2-1 and 2-2 show the clock inputs and outputs on the front and back panels. Tables 2-1, 2-2, 2-3, and 2-4 cover turn on, functional checkout, clock setting procedures, and inputs and outputs.

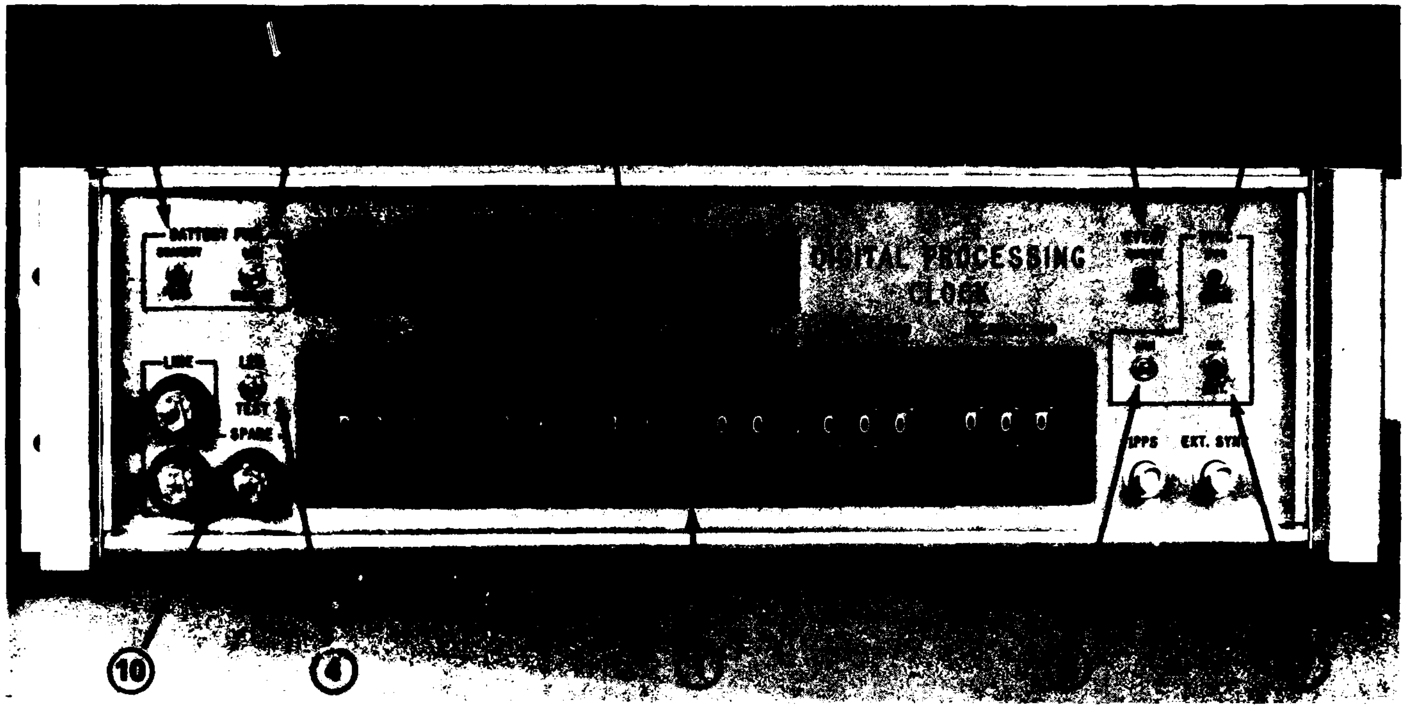
2-1 Turn-On Procedure

Turn on may be accomplished by following the directions in Table 2-1.

TABLE 2-1

TURN-ON PROCEDURE

STEP	OBSERVE	REF
1. Initial Switch Settings Battery Power OFF Event INHIBIT Sync 1 PPS/Clock CLOCK Int/Ext EXT Thumbwheels All "0"	Nothing (Power Off)	Fig. 2-1
2. Connect BNC cable from source of 1 MHz to 1 MHz IN on rear panel of clock	Nothing (Power Off)	Fig. 2-2
3. Attach AC power cable to 3-pin AC Power Input connector reading 115 VAC on rear panel	Nothing (Power Off)	
4. Plug other end of AC Power cable into 115 V 60 Hz source	All LED readouts lit Seconds count advancing each second as clock reads some random time	



1. Thumbwheel Switches—15 unit decade used for time setting, delay insertion, and time of event operations.
2. Battery Standby/Off Switch—in Standby postion supplies backup power for clock for ½ hour; in Off position battery is taken out of circuit to prevent discharging during shipping or storage.
3. LED Display—when on battery power, push to get display of day of year and time of day.
4. LED Test—when pushed display shows all 8s and decimal points lit.
5. Event Output/Inhibit—Time of Event outputs on back of clock are enabled in Output position.
6. Sync 1 PPS/Clock—in Clock position sets clock to time on thumbwheel switches and syncs to within one microsecond with sync signal when it arrives. In 1 PPS position only the subsecond timing is changed.
7. Sync Int./Ext.—in Int. position syncs clock with internally generated 1 PP10S. In Ext. position syncs clock to applied Ext. Sync signal.
8. Sync Arm—push button to arm clock for arrival of sync signal.
9. Display—7 segment LED display of Day, Hour, Minute, Second information and flashing decimal point indicators for (1) clock armed (3 points to left of each day digit), (2) clock on Internal Oscillator (1 point to left of tens of minutes), (3) coincidence of Sync to within one microsecond (2 points to left of second digits).
10. Fuses—two 1.5A Line fuses and one spare.

Figure 2-1—Operator Controls

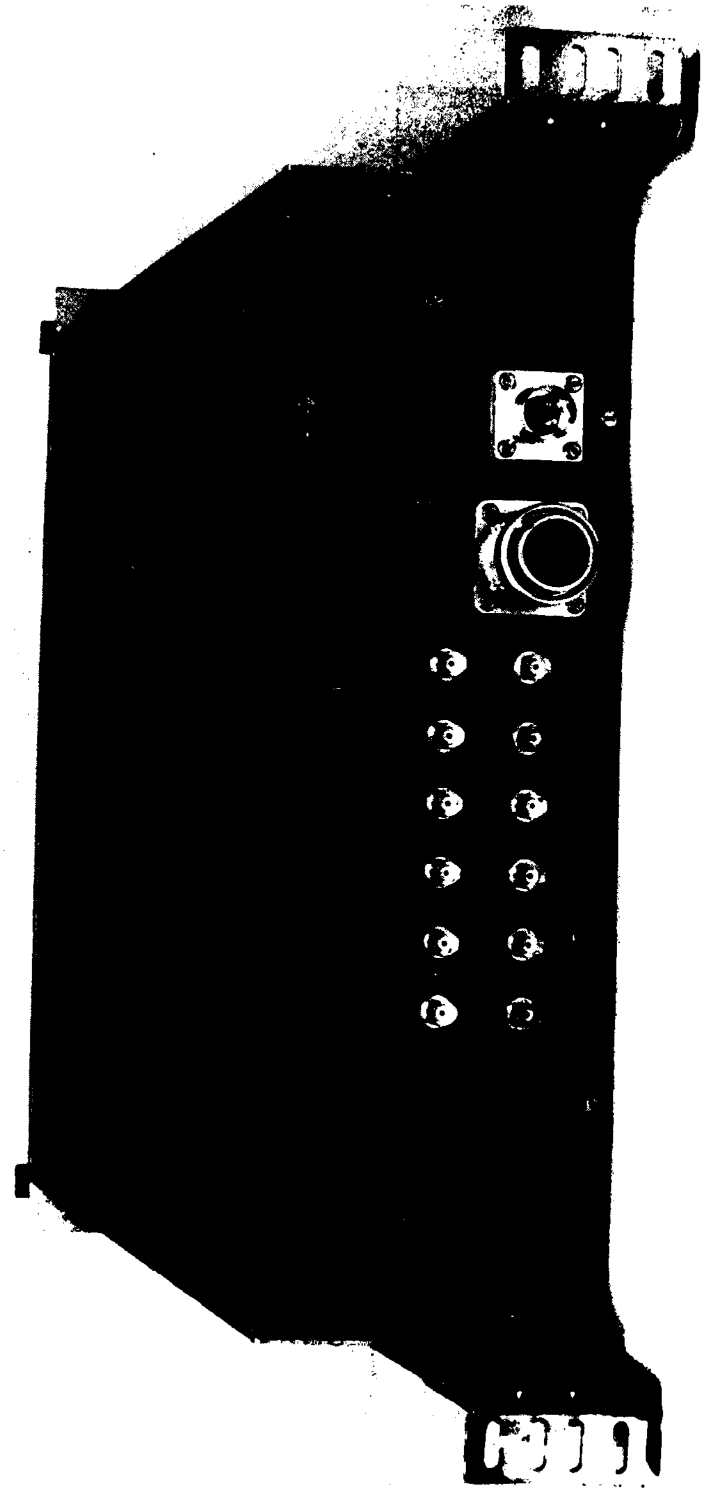


Figure 2-2—Back View of Digital Processing Clock

TABLE 2-1

TURN-ON PROCEDURE—(Continued)

STEP	OBSERVE	REF
5. Switch Sync Int/Ext to INT	Same as above	3-1
6. Depress and release Sync ARM	3 decimal points in Days portion of display light	3-2-3(b)
7. Wait for clock display to make 9 to 0 transition in seconds position	Clock readout sets to all zeros and begins keeping time from that point Decimal point LED's in Days turn off	3-2-4(c) 3-2-5(b) 3-2-3(b)

2-2 Operator Controls

Figure 2-1 shows the operator controls in detail

2-3 Functional Checkout Procedure

Functional checkout is accomplished by following the directions in Table 2-2.

TABLE 2-2

FUNCTIONAL CHECK-OUT PROCEDURE

STEP	OBSERVE	REF
1. Switch Settings Battery Power STANDBY Event INHIBIT Sync 1 PPS/Clock CLOCK Int/Ext EXT Thumbwheels All "0"	Clock operating as described in step 7 of Table 2-1.	Fig. 2-1
2. Depress the LED Test pushbutton on the left side of the clock's front panel	All nine numeric displays indicate 8 and all decimal points are lit	
3. Release LED TEST pushbutton	Clock resumes displaying time information	
4. Disconnect the AC Power cord from its source	Clock display goes blank	

TABLE 2-2

FUNCTIONAL CHECK-OUT PROCEDURE—(Continued)

STEP	OBSERVE	REF
5. Depress and hold LED DISPLAY pushbutton	Time information is displayed on clock readout	
6. Release LED DISPLAY and reapply AC Power	Display is on continuously and without any loss of elapsed time	
7. Connect a BNC cable from the A Time Event Out connector on the rear panel to the Ext Sync input connector on the front panel of the clock	Nothing	Fig. 2-2
8. Place Event switch to the OUTPUT position	Nothing	Fig. 2-1
9. Set thumbwheels to a time slightly *ahead* of the actual time displayed on the clock, keep millisecond and microsecond thumbwheels set to all zeros	Nothing	
10. Wait for the time on the clock display to reach the time set into the thumbwheels in step 9	Seconds display; when clock time agrees with thumbwheel time, 2 decimal points in seconds display should flash once Event circuit is functioning properly	3-2-3(d)
11. Remove BNC cable installed in step 7; connect it between 1 PPS output and Ext Sync input on front panel	2 decimal points in seconds display should be flashing on and off at a once-per-second rate	3-2-3(d)
12. Repeat step 11 for the two 1 PPS outputs and the B Time Event Out output on the rear panel of the clock	Same as for step 11 All 1 PPS output circuits are functioning properly	3-1
13. Remove BNC cable used in step 12 and set all switches to positions specified in step 1	Nothing	

TABLE 2-2

FUNCTIONAL CHECK-OUT PROCEDURES—(Continued)

STEP	OBSERVE	REF
14. Disconnect the 1 MHz Input cable from the rear panel	Decimal point in Tens of Minutes display comes on	3-2-3(c)
	Clock display still advancing at once per second rate with no discontinuity from before cable was removed	3-2-2
15. Reconnect the 1 MHz Input cable to rear panel input jack	Tens-of-Minutes decimal point turns off	3-2-3(c)
	Clock display still advancing at once-per-second rate with no discontinuity when external 1 MHz was reapplied	3-2-2(b)
16. Proceed to Clock Setting Procedure	Table 2-3	

2-4 Clock Setting Procedure

Table 2-3 details the clock setting procedure.

TABLE 2-3

CLOCK SETTING PROCEDURE

STEP	OBSERVE	REF
1. Switch Settings Battery Power STANDBY Event INHIBIT Sync 1 PPS/Clock CLOCK Int/Ext EXT	Clock operating as described in the TURN-ON Procedure	Fig. 2-1
2. Attach BNC cable from source of external sync pulse to EXT SYNC input on front of clock	Same as above	3-1

TABLE 2-3

CLOCK SETTING PROCEDURE—(Continued)

STEP	OBSERVE	REF
3. Set front panel thumbwheels to the arrival time of the *next* external sync pulse Depress the Sync ARM button such that the clock will be in its armed state when the sync pulse arrives (if using external 1 PPS depress Arm Button less than one second before time set in thumbwheel switches)	3 decimal points of Days should light until sync pulse arrives	3-2-3(b)
4. Wait for arrival of external sync pulse	Decimals go out Clock readout changes to agree with thumbwheels and proceeds to keep time from that instant	3-2-3(b) 3-2-4(c)
Note: If in step 3 the arrival time of the external sync pulse was an *integral multiple of a second*, such as a 1 PPS pulse train from an external time source, then observe	2 decimal points in the Seconds and Tens of *Seconds positions in the* readout should flash for about 0.3 seconds each second, indicating that the Ext Input and internal 1 PPS agree to within 1 μs	3-2-3(d)
5. Remove cable from Ext Sync Input jack	All decimal points out Clock indicates correct time in days, hours, minutes and seconds	
6. If no source of external sync pulse is available, the clock may be set to the correct Day of Year and Time of Day with the Sync 1 PPS/CLOCK switch in CLOCK position and the Sync INT/EXT in INT position thus using the internally generated 1PP10S. This requires two steps: (a) Set front panel thumbwheels to Day of Year and correct	Decimal point to left of Tens of Minutes should light and 2 decimal points in Seconds will flash once on the even ten seconds	3-2-3(c)

TABLE 2-3

CLOCK SETTING PROCEDURE—(Continued)

STEP	OBSERVE	REF
Time of Day to the next even minute. Depress the Sync Arm button on the even minute set in the thumbwheel switches such that the clock will be in its armed state when the next internally generated 1PP10S arrives. When the pulse arrives the clock will set itself to the time in the thumbwheel switches and will be from 0 to 10 seconds behind.	3 decimal points of Days display should light until sync pulse arrives 3 decimal points of Days display should go out.	3-2-3(b) 3-2-3(b) 3-2-3(b)
(b) Note the number of seconds the clock is behind. Advance the minute thumbwheel to the next minute ahead and set the seconds thumbwheel to the number of seconds the clock is behind (and sub-second thumbwheels if fractions of a second that the clock is behind is known). Depress Arm button on even minute set on thumbwheels. When the internally generated 1PP10S arrives, the clock will set to the accuracy set on the thumbwheel switches.	3 decimal points of Days display should light until sync pulse arrives 3 decimal points of Days display should go out.	3-2-3(b)

2-5 Inputs and Outputs

Inputs and outputs are described in Table 2-4 and shown in Figures 2-1 and 2-2.

TABLE 2-4

INPUTS AND OUTPUTS

UNIT	INPUTS	OUTPUTS
Digital Processing Clock	1 MHz In—1 V rms sine wave or ± 2 Vpp square wave or 4 V positive going pulse; one input on back panel of clock Fig. 2-2.	1 PPS—TTL compatible, > 4 Vpp without load, > 2 Vpp with 50 Ω load, ~ 20 μs wide, rise time < 70 ns; one output on front of clock (Fig. 2-1); two outputs on back panel of clock (Fig. 2-2).
	EXT SYNC—positive going transistion, TTL compatible 2.4 V—5 Vpp, > 50 ns width, rise time < 100 ns; one input on the front of clock	1 PP10S—TTL compatible, > 4 Vpp without load > 2 Vpp with 50Ω load, ~ 20 μs wide, rise time < 70 ns; one output on back panel of clock (Fig. 2-2).
		Time of Event (TOE) outputs—(1PPDAY, 1PPHR, 1PPMIN, 1PP10S, 1PPS selectable by DIP rocker switches on TOE board) TTL compatible > 4 Vpp without load, > 2 Vpp with 50Ω load, 10 μs wide, rise time < 70 ns; 2 Event outputs on back panel of clock (Fig. 2-2). (A) Event output preset to 1PPDAY (B) Event output preset to 1PPS
		Time Code Out—20 lines of BCD information, multipin connector on back panel of clock—pins 1 and 2 (tens of hours), pins 3-6 (hours), pins 7-9 (tens of minutes), pins 10-13 (minutes), pins 14-16 (tens of seconds), pins 17-20 (seconds), pin 21 (ground).
		Unused Outputs—upper 6 BNC's on back panel of clock (Fig. 2-2).
Remote Display Units	Time Code In—multipin connector J1 on back panel of Remote Display Unit, pins 1 and 2 (tens of hours), pins 3-6 (hours), pins 7-9 (tens of minutes), pins 10-13 (minutes), pins 14-16 (tens of seconds), pins 17-20 (seconds), pin 21 (ground).	Time Code out—multipin connector J2 on back panel of Remote Display Unit, pins 1 and 2 (tens of hours), pins 3-6 (hours), pins 7-9 (tens of minutes), pins 10-13 (minutes), pins 14-16 (tens of seconds), pins 17-20 (seconds), pin 21 (ground).

CHAPTER 3

FUNCTIONAL DESCRIPTION

3-1 Overall Functional Description

Figure 3-1 is a block diagram for the Digital Processing Clock showing signal flow and functional operation and inputs and outputs on front and back of clock. The Digital Processing Clock takes the 1 MHz input signal from a frequency standard, for example a cesium beam standard, and divides it down to produce a one-pulse-per-second (1PPS) output tick and the time-of-day information. Should the external 1 MHz signal disappear from the input, an internal 1 MHz signal generated from an internal oscillator (Figure 6-1A) within the clock itself is automatically applied at the input. The accuracy of this signal, however, is one part in 10^7 over a temperature range of 0°C to 50°C and, therefore, the clock will accumulate time error rapidly when this mode of operation exists. The internal oscillator may be retuned with the screw-covered screwdriver adjustment on the top of the oscillator if the clock gains or loses more than 1 microsecond per second while running on its internal oscillator. Buffered outputs from all dividers in the countdown chain are available internally, and the 20 parallel lines of information containing hours, minutes, and seconds in a binary-coded decimal (BCD) format are fed to a multipin connector (Time Code Out, Figure 2-2) on the rear panel of the clock to drive the remote readout units.

Synchronization, time setting, or both, are accomplished by applying an external positive going transition to the External Sync Input on the front panel (Figure 2-1). With the upper Sync switch on the front panel in the Clock position and the lower Sync switch in EXT position, the clock is armed by pushing the Arm button and will set itself to the day of year and time of day displayed on the thumbwheel switches and will

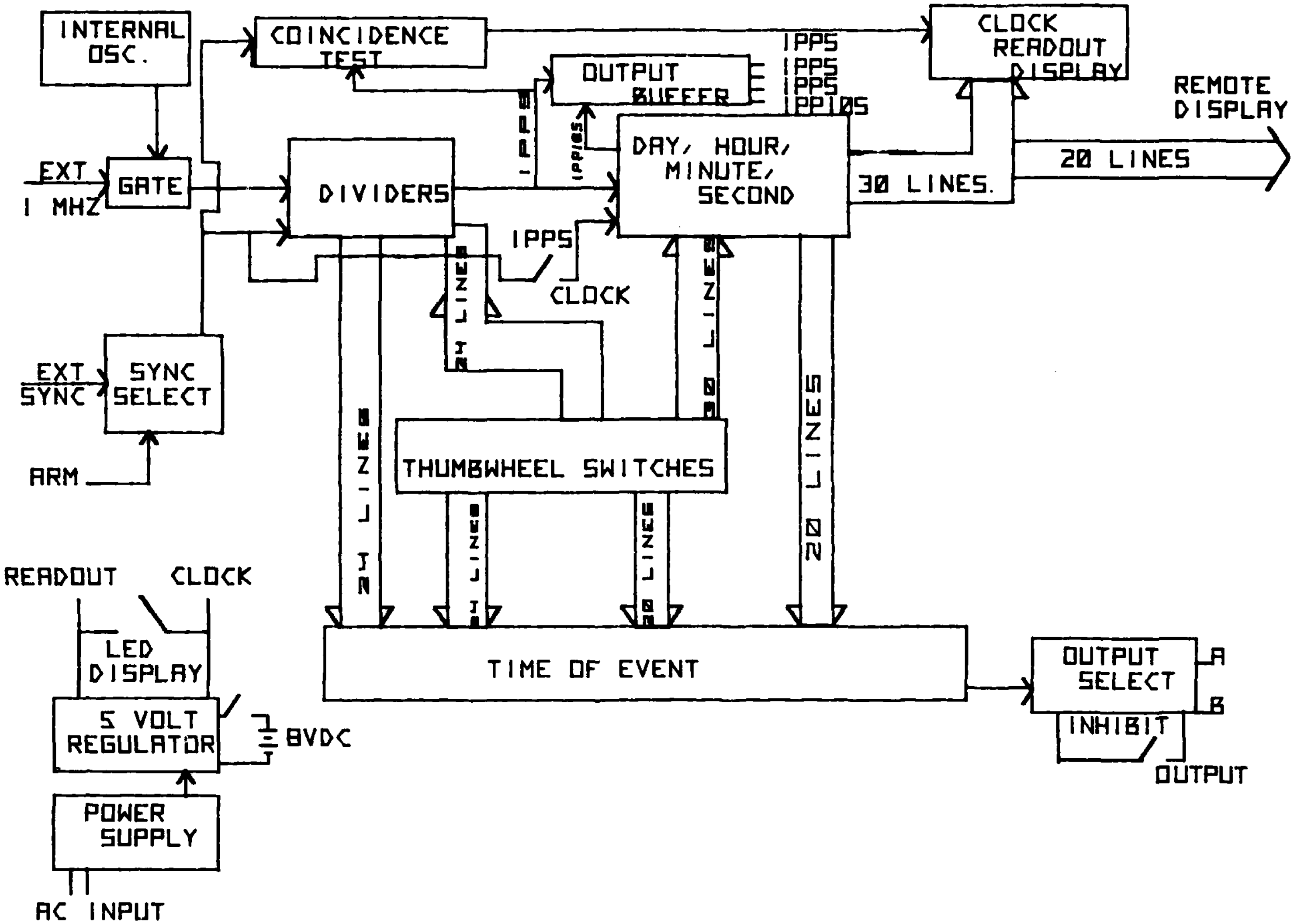


Fig. 3-1—Block Diagram for Digital Processing Clock

synchronize its 1 PPS signal to within one microsecond with the incoming positive going transition when the synchronizing signal arrives if the subsecond thumbwheel switches on the front panel are set to zero. If no external time signal is available, the lower Sync switch on the front panel can be put in the INT position and after the Arm button is pushed the next internally generated (1-pulse-per-10-s) 1PP10S signal will set and synchronize the Digital Processing Clock as described for an external synchronizing signal. With the upper Sync switch on the front panel in the 1 PPS position, one can synchronize only the subsecond timing; the day of year, hours, minutes, and seconds will not be affected.

An output pulse may be generated at any time desired with the Time-of-Event (TOE) output. There are two TOE output BNCs, A and B, on the back of the clock (Figure 2-2). The repetition rate of this event pulse is internally selectable at five different rates (1 PPS, 1 PP10S, 1PPM, 1PPHR, and 1PPDAY) with DIP packaged rocker switches on the TOE Circuit Board (Figure 6-4A). Before shipping, the A switch was set to 1 PPDAY and the B switch to 1 PPS. For the A output (switch A set to 1 PPDAY) when the time of day (Hours, Minutes, Seconds, Milliseconds and Microseconds) as kept by the clock agrees with preset time on the thumbwheel switches, a 10 microsecond wide pulse is generated, provided the event circuit has been enabled by placing the Event Switch to Output position on the front panel (Figure 2-1). For the B output (switch B set to 1 PPS) a 10 microsecond wide one pulse per sec (1 PPS) output can be delayed by the time set up on the subsecond (Millisecond and microsecond) thumbwheel switches on the front of the clock. If the subsecond thumbwheel switches were set to zero, this 1 PPS signal would be synchronized with the 1 PPS output signal available on the front panel.

The Digital Processing Clock normally receives its power through the three-conductor power cable terminated in a polarized three-prong male connector connected to an external power source of 115 V, 60 Hz, single phase. If the power source fails or is disconnected, or the power module develops a fault, the clock is automatically transferred to battery operation with zero time error.

3-2 Major Functional Description

For this description refer to Figure 3-2, a foldout schematic of the overall wiring diagram of the Digital Processing Clock and to the figures referenced by the individual sections.

3-2-1 Power Supply and Battery Functions

(a) The power supply receives 115 V, 60 Hz, single-phase power from an external power source through the external power connector mounted on the back of the clock and the line fuses mounted on the front panel. Following the fuses is an electromagnetic interference (EMI) line filter, which is connected to input terminals of the power supply.

(b) The power supply provides a regulated output of about 9.7 Vdc to the 5 Volt regulator board shown in Figures 6-5A and 6-5B. This board provides two regulated 5 V outputs, one to power the counting and one to power the display functions of the clock. In addition, this circuit provides a constant 9 V to charge the internal battery.

(c) A diode OR gate provides the smooth transfer to battery power in the event that the power supply's output fails. When fully charged the battery should provide standby power for a minimum of ½ hour.

(d) A toggle switch on the front panel allows the battery to be switched into a *Standby* position providing backup power for the clock or into the *OFF* position taking the battery out of the circuit and permitting the clock to be turned off without discharging the battery as for shipping or storage.

3-2-2 Clock Time Base Circuit

(a) The functional job of this circuit is to sense when the external standard signal is applied and to output a 1-MHz square wave to the clock counter, which is de-

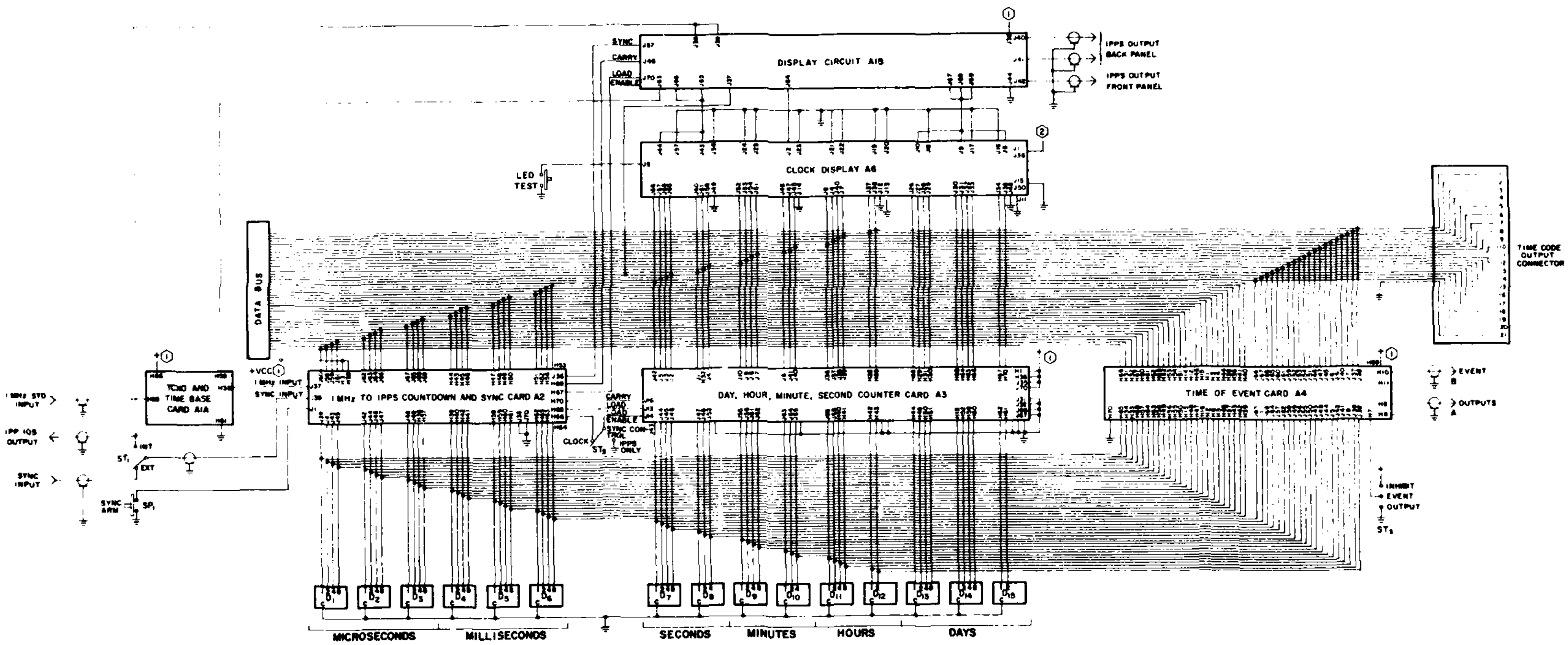


Fig. 3-2 – Wiring Diagram of Digital Processing Clock

rived from this input; if it senses that the external input is not present, this circuit should output a 1-MHz square wave derived from its own internal oscillator.

(b) For the following discussion refer to Figures 6-1A and 6-1B. When an external 1 MHz signal of 1 Vpp or greater is applied to the input (pin 1 of U10), pin 4 of U10 will output a 1 MHz rectangular wave with TTL logic levels. The dc component of this signal charges capacitor C8 such that a high level (H) is produced at pin 5 of U10. This level is inverted to a low level (L) at pin 6 of U10 which disables input pin 4 of U9, the internal oscillator input port. This (L) is again inverted to a (H) and is fed to pin 3 of U9 which enables input pin 2 of U9, the external input port; therefore, the input signal at pin 2 is the only signal allowed by U9 at its output (pin 6). From there the signal is given an approximate 50% duty cycle by one-shot U8, then squared again by schmitt trigger U7, from which it emerges to be sent onto the 1 MHz to 1 PPS Countdown.

(c) When the external 1 MHz signal disappears, capacitor C8 discharges to a (L) and the action of the circuit is reversed in that the internal oscillator port is enabled and the external input port is disabled so that the output of U9 is now derived from the internal oscillator.

3-2-3 Display Circuit Function

(a) In addition to displaying time in days, hours, minutes, and seconds on the nine digit LED display panel, this circuit will indicate (1) when the synchronization circuit is in the armed condition, (2) when the clock is receiving its input from the internal oscillator, (i.e., the external 1 MHz input is off, and (3) when an external pulse applied at the EXT. SYNC input is coincident to within one microsecond of the tick pulse being generated by the clock. Also included on this board are the shaping and driving circuits for the various output pulses of the clock.

(b) For the following discussion refer to Figures 6-1A and 6-1B. The indicator that signifies that the clock has been armed and will set itself with the arrival of the next pulse at the EXT. SYNC INPUT is the lighting of the three decimal point (light emitting diodes) LEDs in the DAYS position of the display panel. When the ARM pushbutton on the front panel is depressed, a (H) load enable is applied to input pin 13 of U6; there it is inverted twice and buffered and fed to three decimal point input pins of the DAYS display. When the synchronization has been acquired, the (L) on the load enable line will turn these three LEDs off.

(c) Should the external standard frequency input be removed or fail, then the (L) from pin 10 of U10 in the Clock Time Base circuit is inverted to a (H) by pins 5 and 6 of U6 and sent to the decimal point input of the TENS of MINUTES display, the fourth digit from the right. When the external standard returns, a (L) applied to this input turns this decimal point LED off.

(d) The coincidence of an externally applied synchronizing pulse with that of the tick pulse generated by the clock is indicated by a pulsing of the two decimal points in the TENS of SECONDS and SECONDS positions. The buffered external synchronizing pulse is applied to input pin 2 of U4, a dual one-shot. The clock's 1 PPS tick is applied to input pin 10 of the second one-shot in U4. Both one-shots respond by outputting strings of one microsecond wide pulses each second from pins 13 and 12, respectively; because pin 12 is a $\overline{Q}$ (not Q) output, this pulse train is inverted. These pulses are fed to the positive and negative inputs of another single monostable circuit U5. Now should the occurrence of both pulses be within one microsecond of each other, U5 will be in an enabled condition and will output a pulse of approximately 0.2 seconds duration. This pulse is fed to the two decimal point displays previously described, causing them to flash on and off each second. If the pulses are more than one microsecond

apart, U5 will never be enabled and, therefore, the decimal point LEDs will always be off.

3-2-4 1 MHz to 1 PPS Countdown and Sync Function

(a) The function of this circuit is to count pulses of the input 1 MHz square wave and produce an output of one-pulse-per-second (1PPS). In addition, the occurrence of this output pulse must be capable of being set to within one microsecond (μs) of any time relative to an externally applied synchronizing pulse.

(b) For the following discussion refer to Figures 6-2A and 6-2B. The 1 MHz square wave is applied to pin 1 of U1, an inverter; the output (pin 4 of U1) is applied to pin 5 of U8, the first decade divider. The output of this counter (now a string of 100 kHz pulses) feeds the input of the next divider U9. This cycle is repeated five more times until one-pulse-per-second (1 PPS) emerges from pin 12 of U13 and enters buffer U6 on pins 1 and 13. The outputs from this buffer (pins 2 and 12) send the 1 PPS information onto the other circuits.

(c) Synchronization of the divider chain is accomplished by applying an external positive going transition to the EXT. SYNC input after the SYNC ARM pushbutton has been depressed. Arming the synchronization circuit, clears flip-flop U3, which enables U2 to respond to the next positive going transition at its input (pin 5). Upon arrival of the synchronizing signal, the divider chain (U8-U13) will set itself in accordance with the binary coded decimal (BCD) information present at its data inputs (pins 15, 1, 10, and 9). The synchronization signal is translated into a very narrow pulse of about 300 ns which emerges from pin 6 of U2; this pulse is gated through the NAND circuits, which have been enabled by cleared flip-flop U3, to the load inputs (pin 11) of all dividers. This

same pulse enters pin 5 of U3 to set the flip-flop, thus inhibiting the 6 NAND gates as well as the one-shot U2; therefore, any more pulses applied to the Ext. SYNC input will have no effect upon the clock's operation. The load pulse from pin 6 of U2 as well as the load enable signal from pin 8 of U3 are also buffered by U6 and sent to other circuits.

(d) All output information (pins 3, 2, 6, and 7 of U3-U13 in BCD form) from the divider chain is buffered by U14-U17 before being sent onto other circuits. Thus, a failure in any circuit that uses this information will not interrupt the counting of the clock's dividers.

3-2-5 Day, Hour, Minute, Second Counter Function

(a) The function of this circuit is to take the 1 PPS signal produced by the circuit described in section 3-3-4 and divide it down further to produce second, minute, hour, and finally, day of the year information, which will be displayed on the clock's front panel.

(b) For the following discussion refer to Figures 6-3A and 6-3B. Operationally, this circuit functions very much like that described in section 3-2-4 in that similar dividers are used while synchronization is accomplished using the information produced by the 1 MHz to 1 PPS Counter. Slight modifications to the counting schemes are employed in some of the counters so that they will count to 6 (U2 and U4) or 24 (U5 and U6) and then reset to zero instead of just straight decade counting. As before, all output information from the dividers is buffered (U10, U12, U14, U17 and U18) before being sent onto other circuits to protect the clocking portion from external disturbances. In addition, all output information from this card is sent to the nine LED displays on the front panel; and the

hour, minute, and second information is also brought out on the rear panel of the clock at the multipin connector (Time Code Out), where it may be used to drive the remote time readouts.

(c) A switch has been installed at the top edge of this card which enables one to modify the feedback loop in the days portion of the counter (U7-U9). In the Regular position the days count will advance up to 365 and reset to 1; in the Leap Year position, the count will go to 366 before resetting to 1. This switch may be changed at any time during the year without affecting the clock's operation.

3-2-6 Time of Event Function

(a) The function of this circuit is to compare the BCD output information from the clock's divider chain with the setting of the digital thumbwheel switches on the front panel. When this comparison indicates total agreement, this circuit should be putting out a 10 μs pulse whose leading edge occurs at the precise time when coincidence was achieved.

(b) For the following discussion refer to the circuit diagram shown in Figures 6-4A and 6-4B. The comparison circuit consists of a string of twelve 4-bit magnitude comparators (U1 through U12). In order that an equality signal (coincidence signal) be generated from any one of the comparators on its output (pin 3), five conditions must be met: (1) a high (H) must be present at the input from the preceding state (pin 6); (2) the 2^0 bits must agree; (3) the 2^1 bits must agree; (4) the 2^2 bits must agree; and (5) the 2^3 bits must agree. Thus, when the time of day agrees with the present time on the front panel thumbwheels, a positive going transition is generated on the output line. This transition is

converted into a 10 μs wide pulse by one-shot U13 and fed to line driver U14, which delivers the pulse to the rear panel BNC output connector.

(c) The repetition rate of the event pulse is internally selectable at five different time intervals: once per second, 10 seconds, minute, hour, and day. For example, if a once per second event output were desired, then only the first six comparators and the six thumbwheel switches on front panel to the right of the decimal point would be used. Each slower repetition rate employs more comparators in the chain and more of the front panel thumbwheel switches. Note that because once per day is the longest time interval available, the three switches at the left which set the days information are not used in conjunction with the TOE circuit.

(d) The EVENT toggle switch available on the front panel is used to enable (OUTPUT) or disable (INHIBIT) the event pulse. This switch places a high (H) disable or a low (L) enable on pins 1 and 9 of U13 to control whether it will respond to the incoming pulses on its inputs (pins 2 and 10).

3-2-7 Remote Display Unit

(a) The Digital Processing Clock System (Figure 1-1) contains four remote display units. Figure 3-3 gives a front view of the display unit and Figure 3-4 gives a back and inside view. The remote display unit which is 35.6 cm (14 in) wide has a simplified design using seven segment on-chip decoders to display the Hours, Minutes, and Seconds.

(b) The wiring from the decoders (TIL 308) to the time code connectors J1 (in) and J2 (out) on the back via the wire wrap socket on the bottom chassis plate is color coded for ease in building, troubleshooting and repair. Figure 3-5 is a

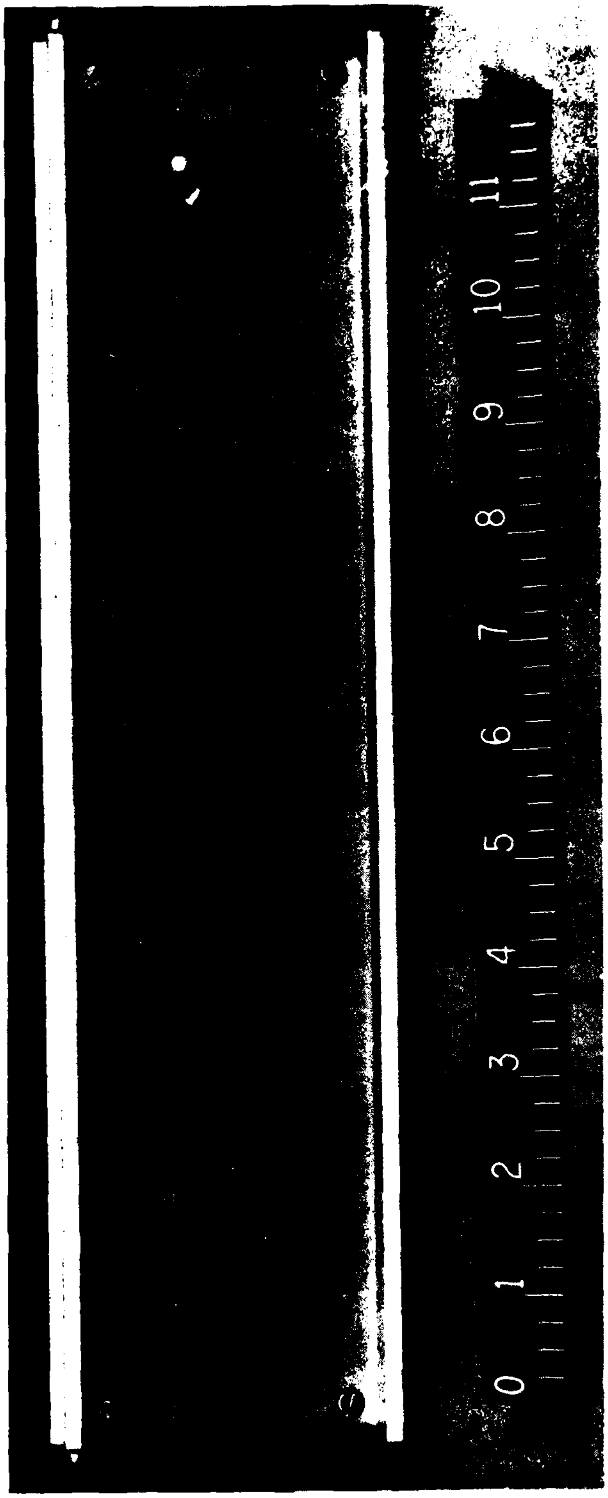


Figure 3-3—Remote Display Unit

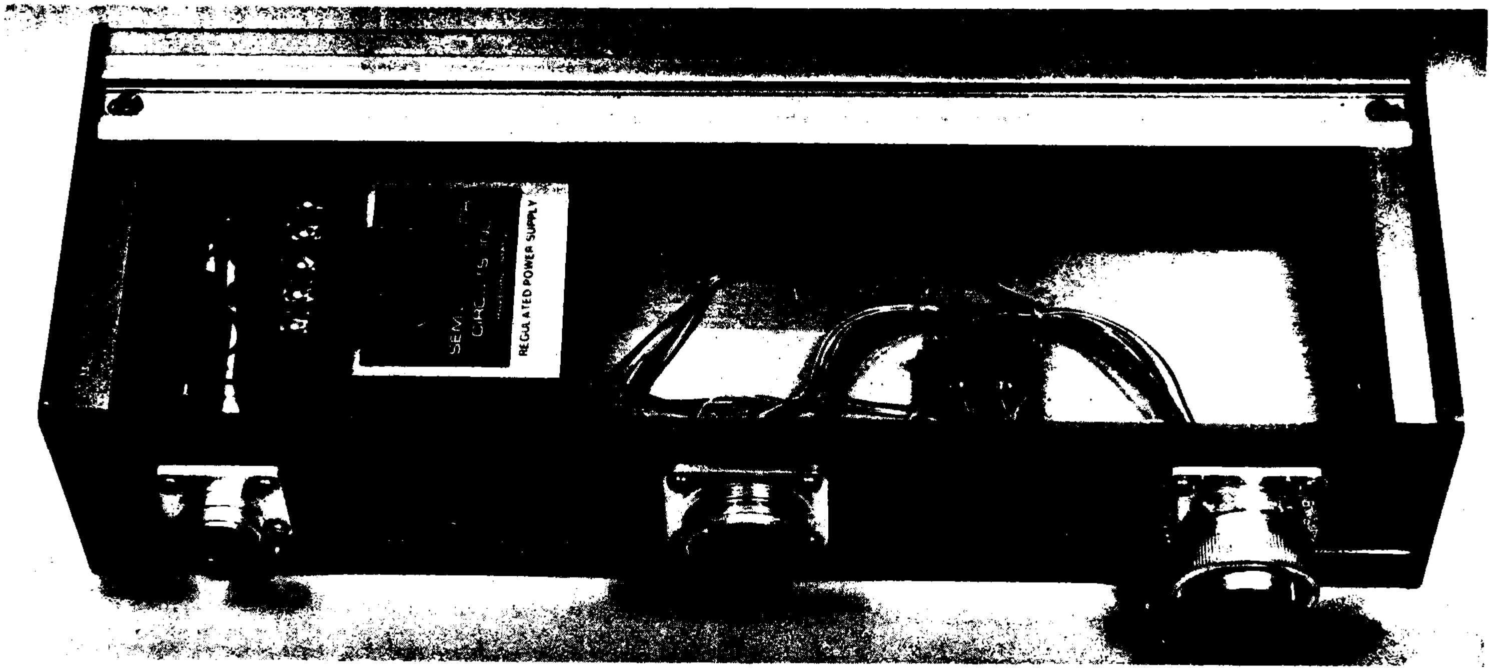


Figure 3-4—Back and Inside View of Remote Display Unit

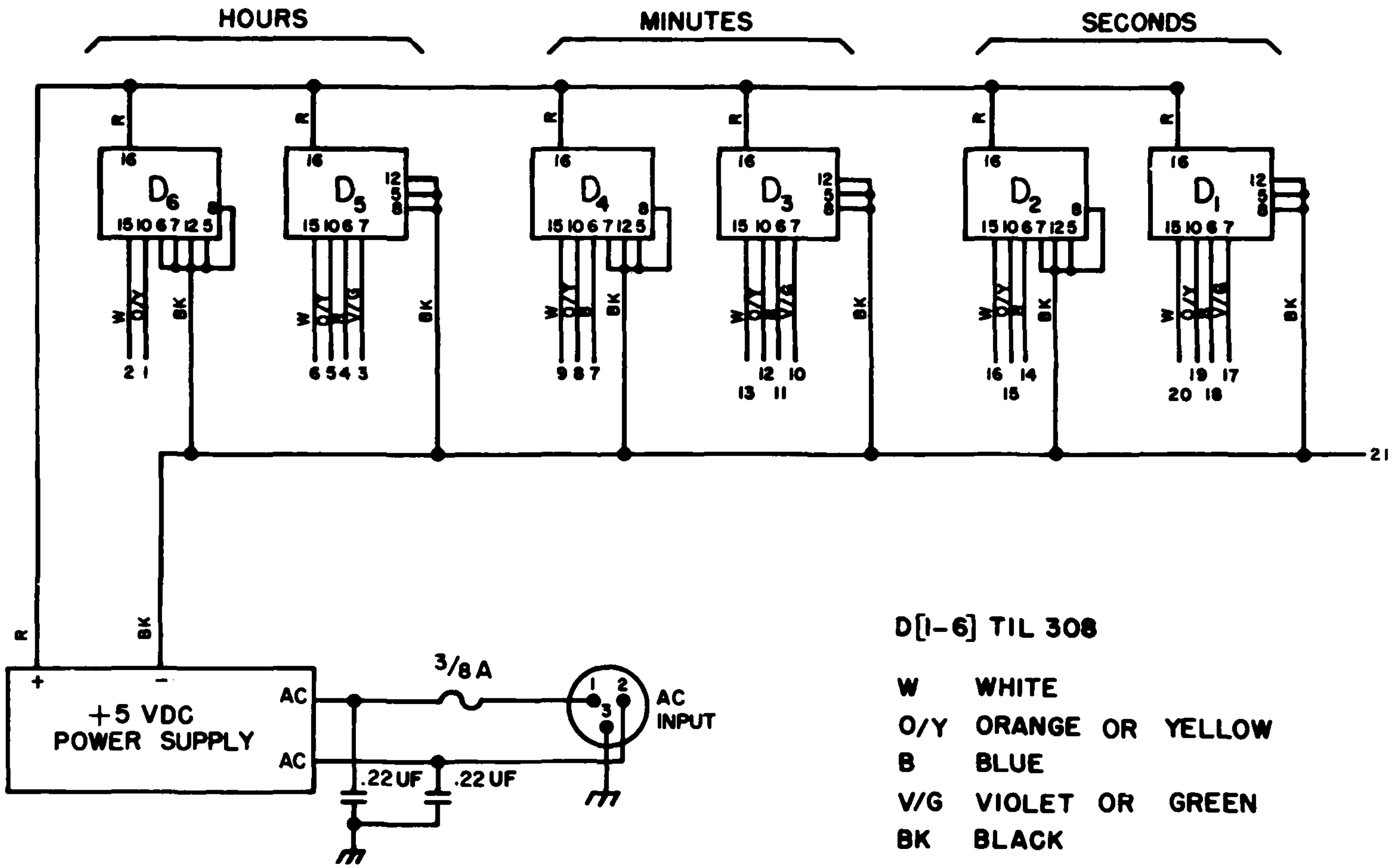


Fig. 3-5—Wiring Diagram of Remote Display Unit

wiring diagram of the remote display unit. The units are powered by a 5 Vdc power supply and fused with a 3/8 A. fuse.

IV. Chapter 4

SCHEDULED MAINTENANCE

4-1 Built-In Test Equipment

The Digital Processing Clock has built-in test equipment (BITE) to ease the checking of proper operation. The status of the BITE indicators should be checked on a regular basis depending on usage. BITE indicators are:

1. LED test—when pushbutton switch on front panel is pushed, the display shows all 8's and decimal points are lit.
2. Flashing decimal point indicators:
   a. Clock Armed (3 decimal points to left of each day digit flash)
   b. Clock on Internal Oscillator (1 decimal point to left of tens of minutes flashes)
   c. Coincidence of Sync to within one microsecond (2 decimal points to left of seconds digits flash).

4-2 Outputs Check

Outputs should be checked to be in accordance with specifications given in Table 2-4. Outputs should always be checked with scope or counter, if possible, before anticipated usage.

4-3 Battery Care

The Digital Processing Clock contains an internal battery pack of sealed Gel Cells (see Figure 4-1) which should provide 1/2-hour of backup power with no time loss in case of

Figure 4-1—Top View of Digital Processing Clock

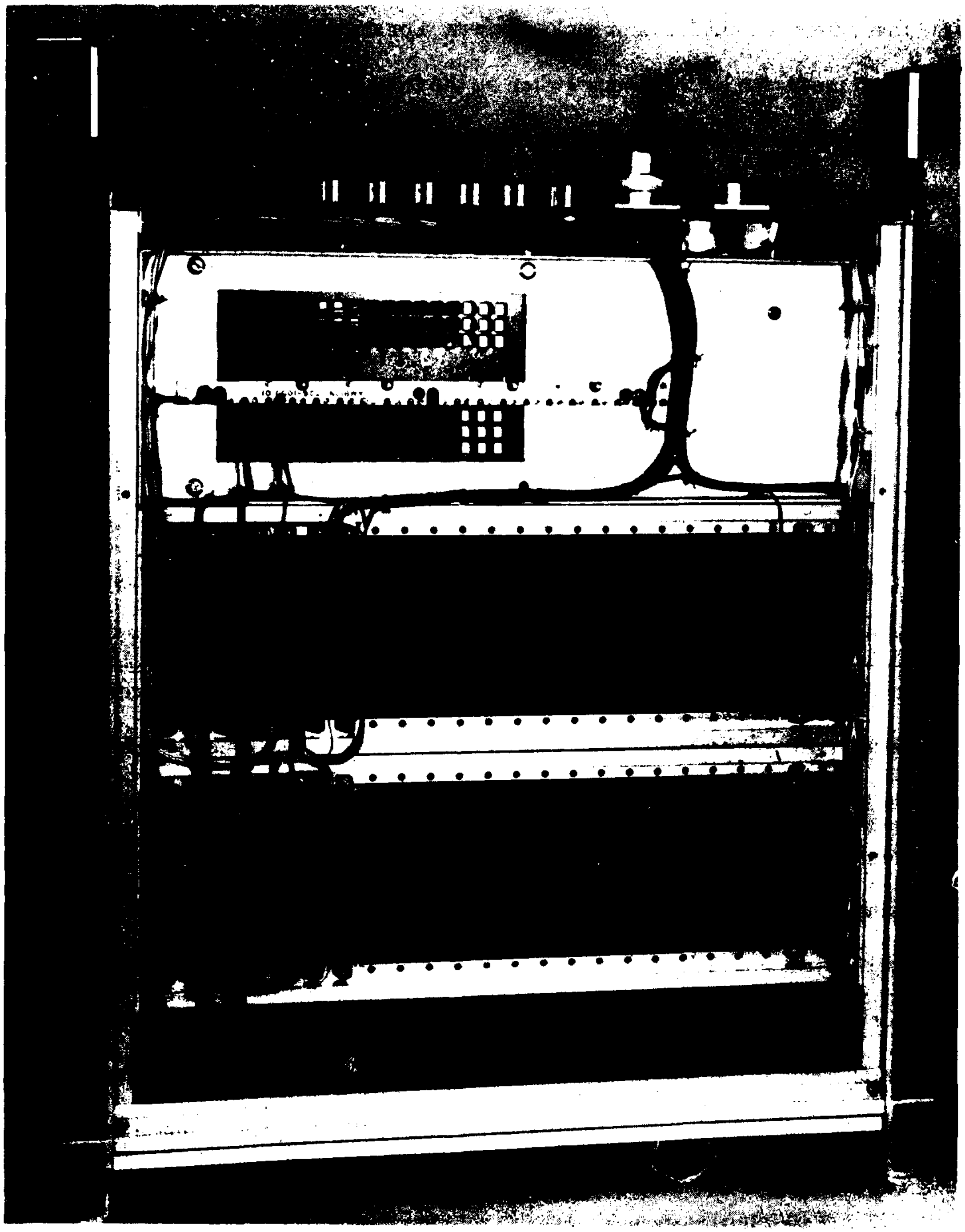


Figure 4-2—Bottom View of Digital Processing Clock

power failure or ship-to-shore switchover. Check periodically when feasible (for example, when a loss of time could be tolerated) to check that clock switches to battery power properly and that batteries yield 1/2 hour backup power. For shipping or storage or standing in a power-off mode, the battery toggle switch on the front panel of the clock should be placed in the *OFF* position to prevent discharging of the battery.

4-4 Leap Year Adjustment

A switch has been installed at the top edge of the Day Hour Minute Second Counter Board (see Figures 4-1 and 6-3A) which enables one to modify the feedback loop in the days portion of the counter. In the Regular position the days count will advance up to 365 and reset to 1; in the Leap Year position, the count will go to 366 before resetting to 1. This switch may be changed at any time during the year without affecting the clock's operation. Because 1976 is a leap year, the clock has been shipped with the switch in the Leap Year position. Any day in 1977, the switch can be returned to the Regular position.

4-5 Time of Event Pulse Selection

Time of Event (TOE) outputs A and B can be programmed independently with dual in-line package (DIP) rocker switches located on the top of the TOE Board (see Figures 4-1 and 6-4A) to give 1 PPDAY, 1 PPHR, 1 PPMIN, 1 PP10S, or 1 PPS in accordance with specifications in Table 2-4.

4-6 Checking Internal Oscillator Drift

The drift of the internal oscillator should be checked if a precision external clock is available for comparison of time accumulation when the Digital Processing Clock is running on its internal oscillator. If the Digital Processing Clock is gaining or losing 1 microsecond per second or 1 second in 11.5 days, the frequency error of the internal oscillator is 1 part in 10^6. The accuracy of the internal oscillator should be 1 part in 10^7 and can be retuned with the screw covered screwdriver adjustment on the top of the oscillator (see Figure 6-1A) to this accuracy provided one has a counter with time interval head available.

CHAPTER 5

TROUBLESHOOTING

5-1 Overall Checks

Troubleshooting the Digital Processing Clock is basically by process of elimination. Once the symptom is recognized, the faulty circuit can be localized and the defective component or circuit board replaced.

In the event of a mulfunction, first check the line fuses on the front panel of the unit. If either neon lamp is glowing, replace its fuse. Check to insure that the unit is connected to a correct ac power source (see specifications 1-3-2.4) and is properly grounded.

Check the +9.7 Vdc output of the power supply to ensure that it is within the rated tolerances (±0.2 V). If adjustment is required, use small screwdriver to adjust the fine voltage control potentiometer marked "Voltage" located above the negative (−) dc output terminal of the supply. The other control marked "Adjust" is for coarse voltage adjustments.

Check the +5.0 Vdc outputs of the regulator board at their output connector pins A5J37 and A5J60, which are readily accessible from the underside of the clock. Both voltages should be within ±0.1 volt.

5-2 Troubleshooting Table

Table 5-1 and the schematics in Chapter 6 are aids for localizing a faulty circuit and correcting the malfunction.

TABLE 5-1

TROUBLESHOOTING

Symptom	Procedure	Notes	Remedy
Initial Conditions: Battery Power OFF; Event INHIBIT; 1 pps/Clock CLOCK; Int/Ext EXT; Thumbwheels ALL "0"; 1 MHz STANDARD APPLIED TO BACK PANEL INPUT JACK			
No LED display; No output voltages	Place battery power switch to STANDBY and press LED DISPLAY push button	LED display appears and output voltages are present. Possible causes: (1) AC power is not applied properly; (2) Line fuses blown; (3) Power supply malfunction; (4) Line filter malfunction	(1) Apply 117 Vac 60 Hz power to AC input; (2) Check neon lamps on fuse holders, replace fuses as indicated
	With power applied at AC input measure voltage at input terminals of power supply. If proper AC voltage is present, line filter is operating properly	No AC voltage at power supply terminals	Replace line filter
	Remove regulator and A5, measure DC output of power supply. If +9.7 volt output present, power supply is operating properly	No DC output from power supply with AC applied at input; power supply has internal failure	Replace power supply and adjust output to rated value
	If power supply is operating properly replace regulator card A5 and remove cards A1, A2, A3 and A4. Measure +5 Vdc outputs at A5J37 and A5J60	Display should now light and indicate .3.F.F 3F .7F .7.F; anything else means a failure in one of the LED's. Outputs should be +5.0 ± 0.1 Vdc	Replace necessary LED. Replace A5 if output incorrect

TABLE 5-1

TROUBLESHOOTING—(Continued)

Symptom	Procedure	Notes	Remedy
Initial Conditions: Battery Power OFF; Event INHIBIT; 1 pps/Clock CLOCK; Int/Ext EXT; Thumbwheels ALL "0"; 1 MHz STANDARD APPLIED TO BACK PANEL INPUT JACK			
	Plug in cards A1 through A4, starting with A1, one at a time until malfunction occurs	After A1 returned, display should be .3.F.F 3 F 7 F 7 F. After A2 returned, display should be 3 F F 3 F 7 F 7 F and 1 PPS outputs should be present. After A3 returned, display should be some random time and be advancing in 1 sec steps; the 1 PP10S should also return. After A4 returned, event outputs should be present	When malfunction occurs, replace card causing malfunction
Seconds do not advance	Check pin A1H36 for presence of 1 MHz square wave	The 1 MHz signal should be 4 Vpp.	If no 1 MHz waveform present, replace card A1
	Using logic probe check pin A2H70 for the presence of once per second tick pulse	Probe will flash at a once per second rate	If no pulse occurs, replace card A2
	Using logic probe check A3J16 for the presence of the 1 PPS tick pulse	Probe should flash at once per second rate	Wire connecting A2H70 and A3J16 faulty if no tick pulse at A3J16
	Check pins A3 (J42, 5, 3, 2) for the proper BCD voltage levels	J42 is the 2^0 bit; J5 is the 2^1 bit; J3 is the 2^2 bit; J2 is the 2^3 bit of the seconds information	If these levels are not correct, replace A3

TABLE 5-1

TROUBLESHOOTING—(Continued)

Symptom	Procedure	Notes	Remedy
Initial Conditions: Battery Power OFF; Event INHIBIT; 1 pps/Clock CLOCK; Int/Ext EXT; Thumbwheels ALL "0"; 1 MHz STANDARD APPLIED TO BACK PANEL INPUT JACK			
Seconds, minutes hours, or days do not count properly	Check the +5 V output of clock regulator A5U2 at pin A5J60	Should be within tolerance of ±0.1 V	Replace board A5 or the regulator U2 if voltage not correct
	With logic probe check pin A3J16 for the presence of 1 PPS tick	Probe light should flash only once per second, no more or less	If input to A3J16 is correct, replace A3
No output from 1 PPS or 1 PP10S	Using logic probe check A1J46 for presence of 1 PPS and A1J37 for presence of 1 PP10S		If these signals are present, replace A1
No output from time of event	Place Event switch on front panel to the OUTPUT position	Event output circuit is now enabled and event output should be available at each of the output terminals on back panel	
	If Event outputs are still not present, remove top cover and check that one and only one switch in A4S1 and A4S2 is in ON position and the rest are in OFF position	Event output pulses of 10 μs duration should now appear at the time set on the front panel thumbwheels. If no event outputs are observed:	Replace card A4
Clock loses time when AC power is interrupted	Remove AC power from clock; press LED DISPLAY pushbutton	Clock display should light showing time of day. If display is dark proceed:	
	Using a voltmeter measure the DC voltage at A5H36	If the voltage is at its nominal level of +8 volts:	Diode A5D4 is open and should be replaced

TABLE 5-1

TROUBLESHOOTING—(Continued)

Symptom	Procedure	Notes	Remedy
Initial Conditions: Battery Power to STANDBY; Event INHIBIT; 1 pps/Clock CLOCK; Int/Ext EXT; Thumbwheels ALL "0"; 1 MHz STANDARD APPLIED TO BACK PANEL INPUT JACK			
		If the voltage is zero or close to it:	Battery is in discharged condition. Apply AC power to clock and allow 24 hours for battery to recharge
	After 24 hours of charge (Battery Power switch still in STANDBY) disconnect AC power and depress LED DISPLAY pushbutton	Display should now light and time should be continuous from that time on the clock before the power was removed. If display is dark:	Battery is defective and should be replaced
Initial Conditions: Same as above; connect clock to remote readout using 21 wire cable.			
Remote display not functioning	Check to see that cable between clock and remote readout is attached properly; apply AC power to remote readout at J3; press front panel Power switch on readout	Remote readout should now be displaying the same time of day in hours, minutes, and seconds as displayed by the clock	
	Remove the top cover of the remote readout; using an AC voltmeter, measure the AC voltage between the 2 AC terminals of the power supply	If no AC voltage appears across AC terminals:	Line fuse is probably blown and should be replaced with a 3/8-amp slow-blow fuse
		If nominal 117 V AC is present, measure 5 V power supply output with DC voltmeter. If voltage is other than +5 V ± 0.2 V:	Replace power supply

TABLE 5-1

TROUBLESHOOTING—(Continued)

Symptom	Procedure	Notes	Remedy
Initial Conditions: Battery Power to STANDBY; Event INHIBIT; 1 pps/Clock CLOCK; Int/Ext EXT; Thumbwheels ALL "0"; 1 MHz STANDARD APPLIED TO BACK PANEL INPUT JACK			
		If fuses continue to blow when replaced, disconnect the 2 line filter capacitors from the AC terminals. If this cures the problem:	Replace the line filter capacitors
Display of remote readout not indicating time properly	With remote readout turned on and AC power properly applied, remove the cable connecting the clock and remote readout from input connector J1	The display of the remote readout should now indicate anything other than this:	Remove the LED display and replace those readouts that show the incorrect characters.
	Attach input cable to connector J1 on back of remote readout.	Check the spacing of the 24 pin wire wrap terminals inside the remote readout.	Make sure that none of the terminals have been bent so as to short circuit to one another
	If the above have failed to correct the problem, refer to the wiring diagram of the remote readout, Figure 3-5	Using a logic probe, note the voltage levels of the incoming timing information for the LED that are not indicating properly. If errors are detected, remove output cable from the clock and check the Time Code Output connector for the same errors. If the errors are not present at the clock's output:	Cable connecting the clock and remote readout must be wired incorrectly

CHAPTER 6

CORRECTIVE MAINTENANCE

6-1 Overall View

Except for the power supply and battery, the equipment is of modular construction, using plug-in repairable circuit boards designed on a functional basis. For the most part, corrective maintenance will consist of determining which board has caused the failure or problem by using the Troubleshooting table, Table 5-1 of Chapter 5 and replacing the bad board with a replacement board. Section 6-3 contains schematics and part location indexes for the five plug-in boards of the Digital Processing Clock. Spare cards can be stored in the card bucket of the clock.

6-2 Card Replacement

To order replacement cards for the Digital Processing Clock, use the following identification number stamped on the boards:

Clock Time Base and Display Circuit Board: NRL 184-1-A1A and NRL 184-1-A1B

1 MHz to 1 PPS Countdown and Sync Circuit Board: NRL 184-1-A2

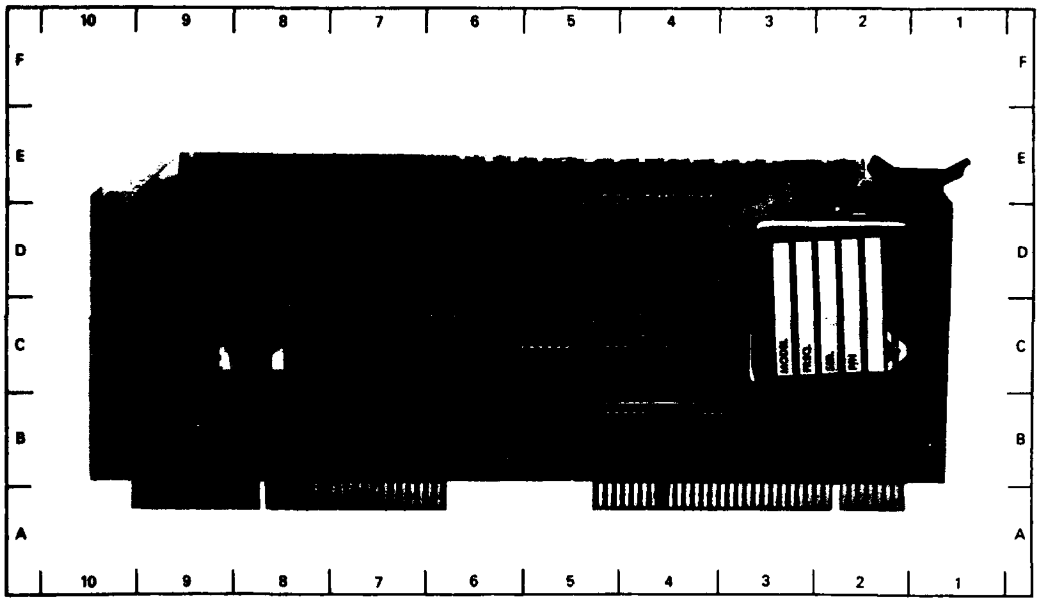
Day Hour Minute Second Counter Board: NRL 184-1-A3

Time of Event Circuit Board: NRL 184-1-A4

5 Volt Regulator Board: NRL 184-1-A5

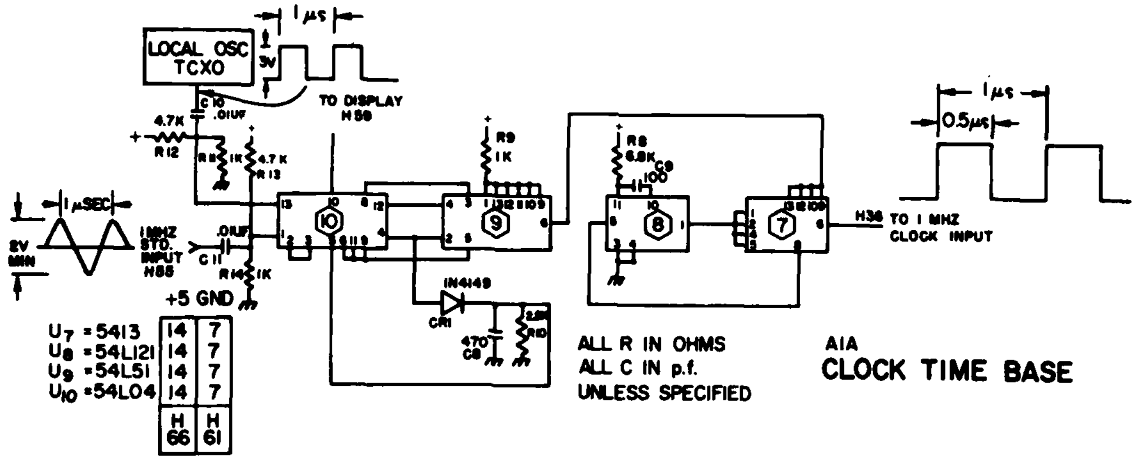
6-3 Schematics and Part Identification

Figures 6-1B, 6-2B, 6-3B, 6-4B and 6-5B are schematics of the five plug-in boards. Figures 6-1A, 6-2A, 6-3A, 6-4A, and 6-5A are photographs with part location indexes of the five plug-in boards. They are arranged in this order to facilitate coordinating the schematics with the actual physical parts.



Reference Designation	Location	Reference Designation	Location	Reference Designation	Location	Reference Designation	Location
A1BC1	D9	A1BR4	C7	A1AC9	C4	A1AR13	B2
A1BC2	C9	A1BR5	C7	A1AC10	B3	A1AR14	B2
A1BC3	C8	A1BR6	C6	A1AC11	B3	A1AU7	C5
A1BC4	C7	A1BU1	D10	A1ACR1	B4	A1AU8	C4
A1BC5	C6	A1BU2	C10	A1AR7	removed	A1AU9	B5
A1BC6	C7	A1BU3	C9	A1AR8	C4	A1AU10	B4
A1BC7	C6	A1BU4	C8	A1AR9	B5	A1AY1	C3
A1BR1	D9	A1BU5	C7	A1AR10	B4		
A1BR2	C9	A1BU6	C6	A1AR11	B2		
A1BR3	C8	A1AC8	B4	A1AR12	B2		

Figure 6-1A—Parts Location Index: Clock Time Base and Display Circuits, Subassemblies A1A and A1B



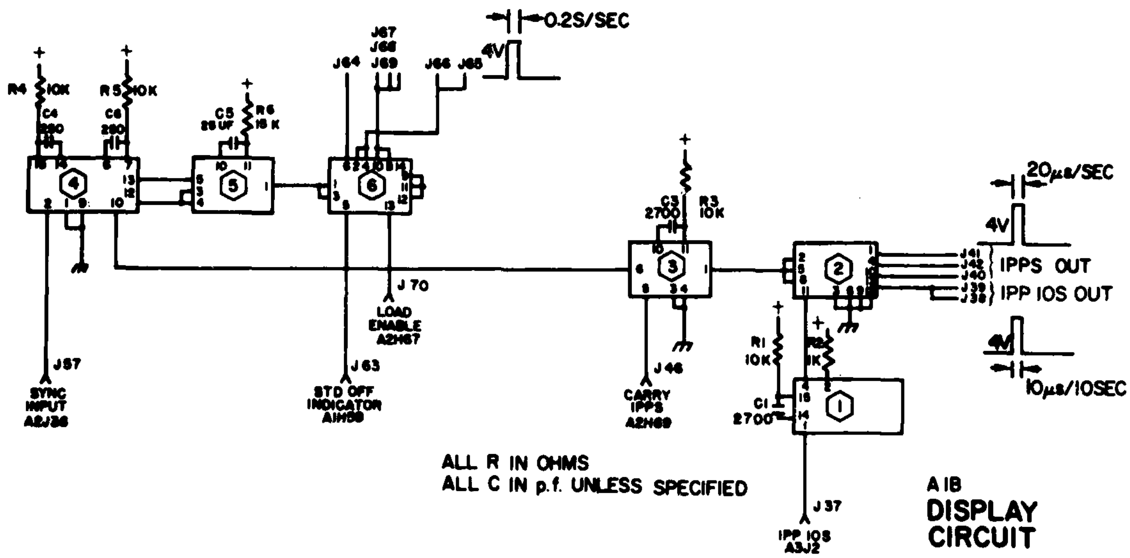
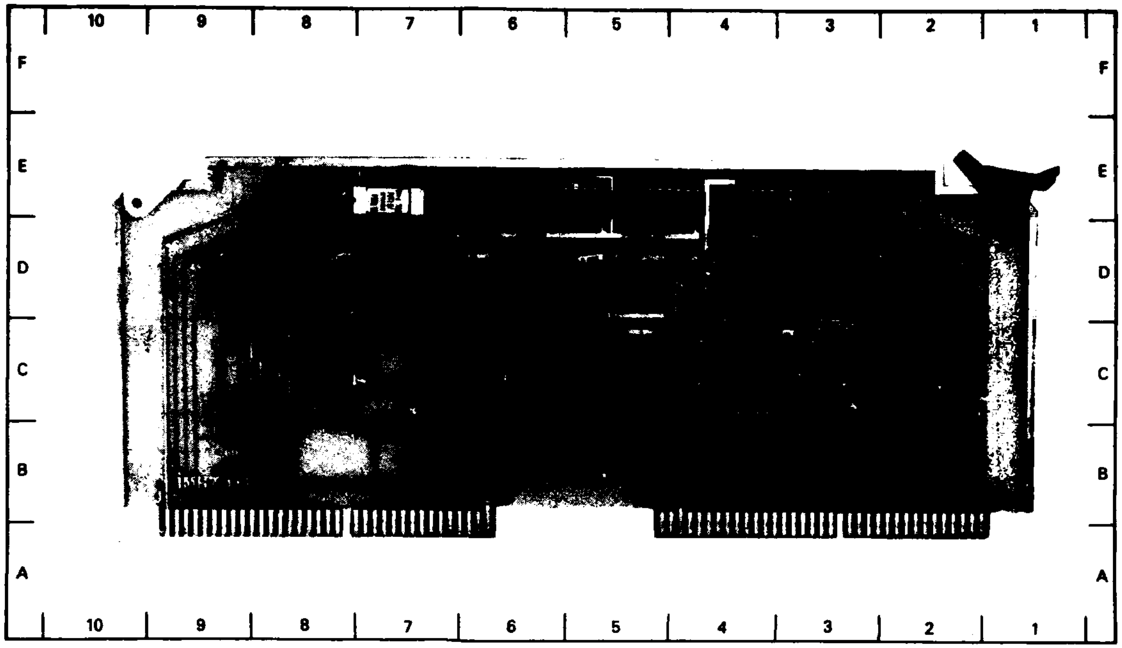


Figure 6-1B—Schematic of Clock Time Base and Display Circuit (see drawings)



Reference Designation	Location	Reference Designation	Location	Reference Designation	Location	Reference Designation	Location
A2C1	D8	A2R4	E6	A2U3	E7	A2U13	D3
A2C2	E7	A2R5	D9	A2U4	E6	A2U14	C8
A2C3	E7	A2R6	D8	A2U5	E5	A2U15	C7
A2C4	D4	A2R7	D7	A2U6	E4	A2U16	C5
A2C5	C6	A2R8	D6	A2U7	E3	A2U17	C3
A2C6	C3	A2R9	D4	A2U8	D9	A2U18	B9
A2R1	D9	A2R10	D3	A2U9	D8	A2U19	B7
A2R2	E8	A2U1	E9	A2U10	D6	A2U20	B6
A2R3	E6	A2U2	E8	A2U11	D5	A2U21	B4
				A2U12	D4	A2U22	B3

Figure 6-2A—Parts Location Index: 1 MHz to 1 PPS Countdown and Sync Circuit Assembly A2

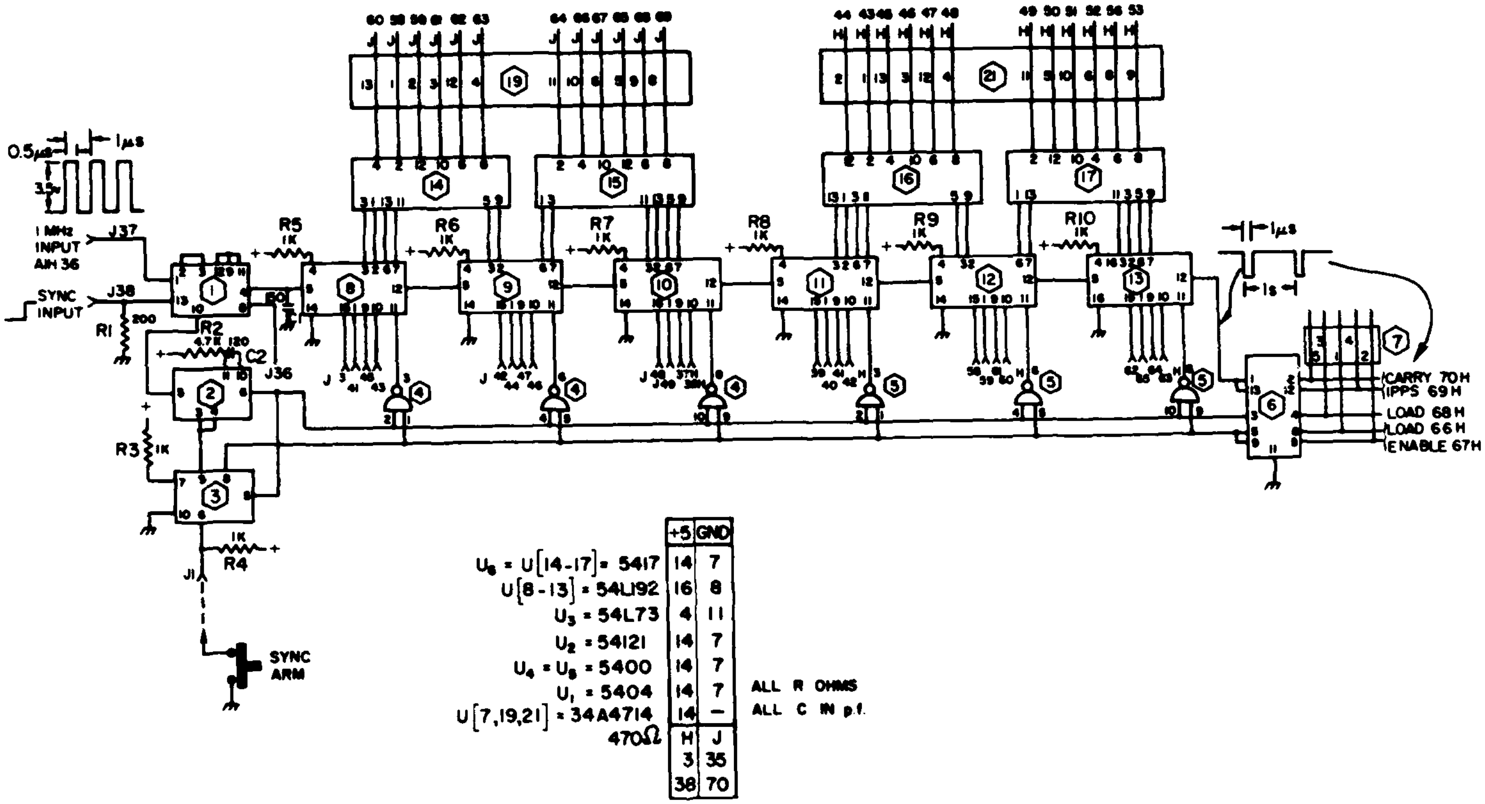
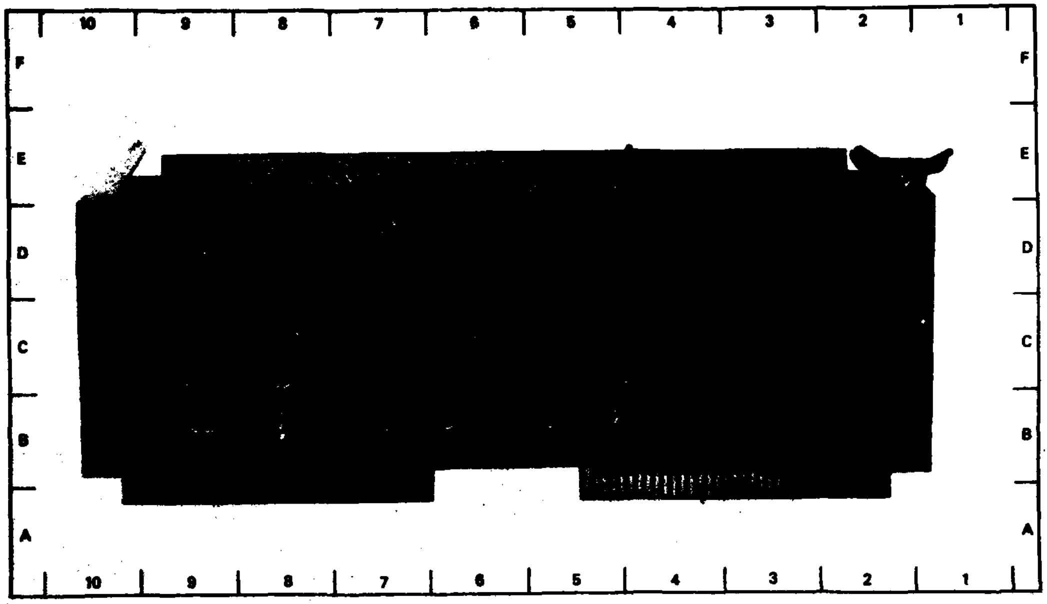
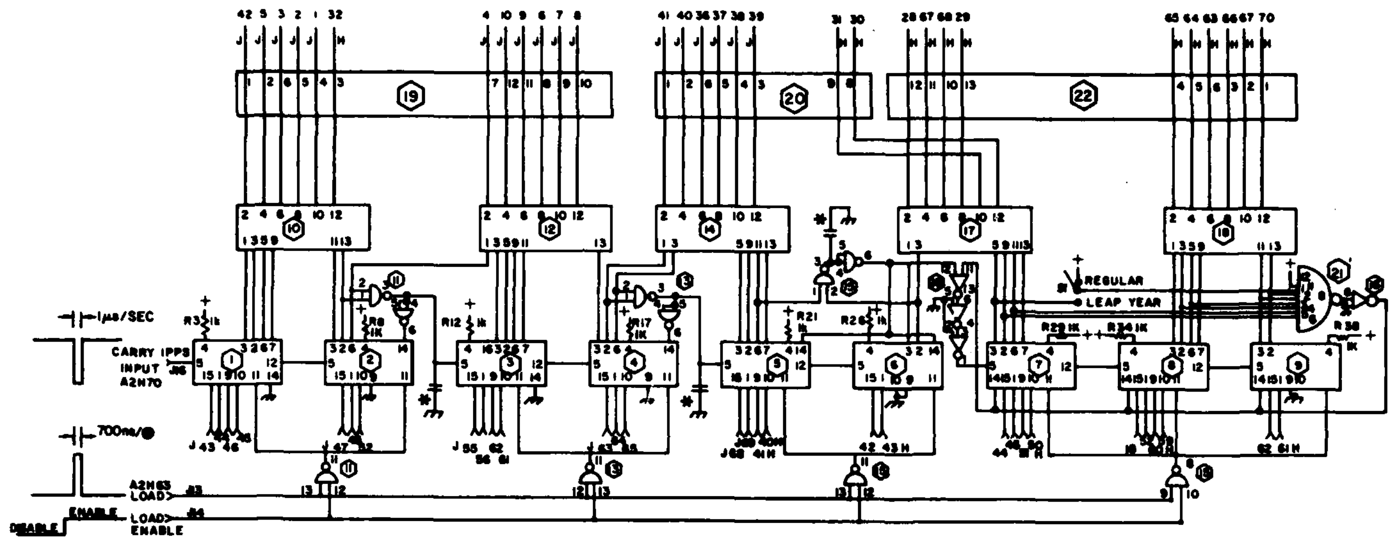


Figure 6-2B—Schematic of 1 MHz to 1 PPS Countdown and Sync Circuit (see drawings)



Reference Designation	Location	Reference Designation	Location	Reference Designation	Location	Reference Designation	Location
A3C1	B8	A3R8-R11	B8	A3U3	C8	A3U13	D7
A3C2	B8	A3R12-R16	B7	A3U4	C7	A3U14	D6
A3C3	B4	A3R17-R21	B6	A3U5	C6	A3U15	D5
A3C4	B4	A3R22-R26	B5	A3U6	C5	A3U16	D4
A3C5	C7	A3R17-R31	B4	A3U7	C4	A3U17	D3
A3C6	C4	A3R32-R36	B3	A3U8	C3	A3U18	D2
A3C7	Individually	A3R37-R39	B2	A3U9	C2	A3U19	D9
A3C8	selected if	A3S1	E4	A3U10	D10	A3U20	D6
A3C9	needed (row C)	A3U1	C10	A3U11	D9	A3U21	D3
A3R1-R2	B10	A3U2	C9	A3U12	D8	A3U22	D2
A3R3-R7	B9						

Figure 6-3A—Parts Location Index: Day Hour Minute Second Counter Assembly A3



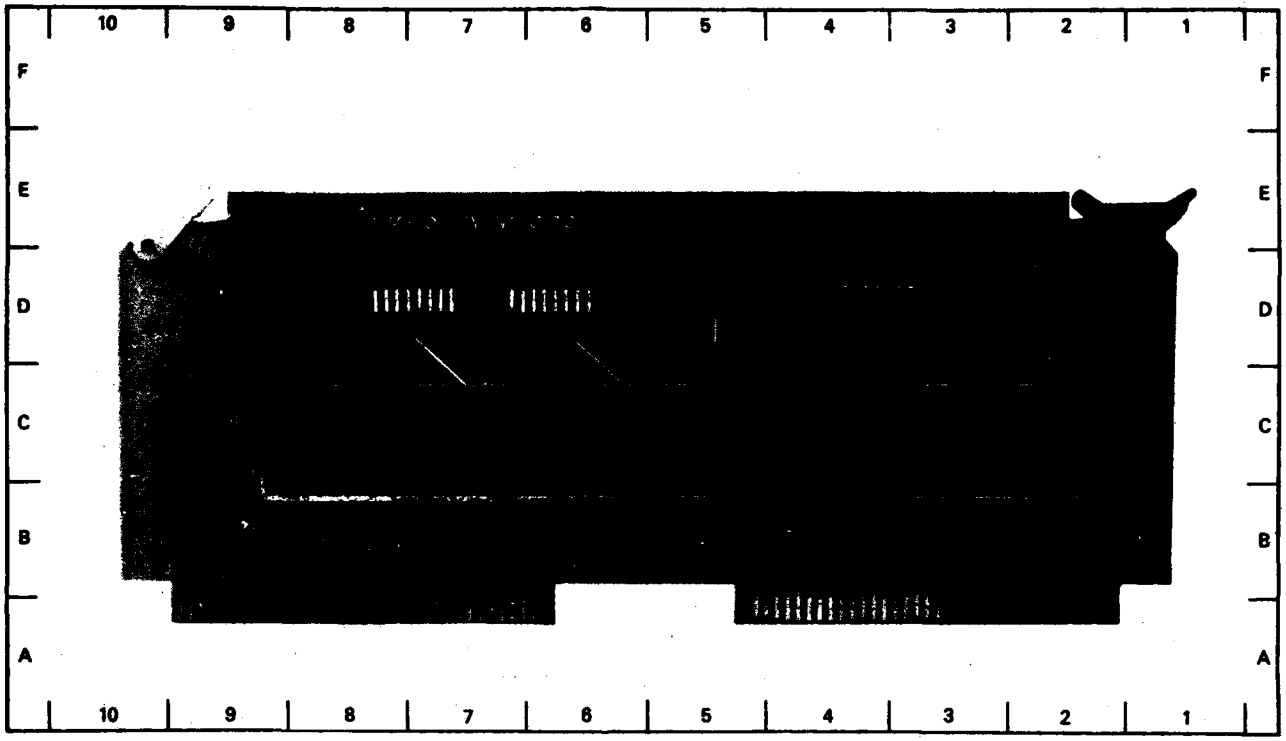
*USED TO WIDEN
CARRY PULSE IF NEEDED
150p.f. TYPICAL

⊛OCCURS ONLY ONCE
AFTER ARM IS PUSHED

	5	[illegible]
U[10,12,14,17,18] = 5417	14	7
U[1-9] = 54L192	16	8
U_{21} = 54L30	14	7
U_{16} = 54L02	14	7
U[11,13,15] = 54L00	14	7
U[19,20,22] = 34A4714 470Ω	14	–
	J 35 70	J 66 67

ALL R IN OHMS
ALL C p.f.

Figure 6-3B—Schematic of Day Hour Minute Second Counter Circuit (see drawings)



Reference Designation	Location	Reference Designation	Location	Reference Designation	Location	Reference Designation	Location
A4C1	B9	A4R1	B2	A4U3	C8	A4U10	C3
A4C2	B5	A4R2	E5	A4U4	C7	A4U11	C2
A4C3	B1	A4R3	D5	A4U5	C7	A4U12	C1
A4C4	B1	A4S1	D8	A4U6	C6	A4U13	D4
A4C5	D5	A4S2	D7	A4U7	C5	A4U14	D3
A4C6	D5	A4U1	C9	A4U8	C5		
A4C7	D4	A4U2	C9	A4U9	C4		

Figure 6-4A—Parts Location Index: Time of Event Circuit Assembly A4

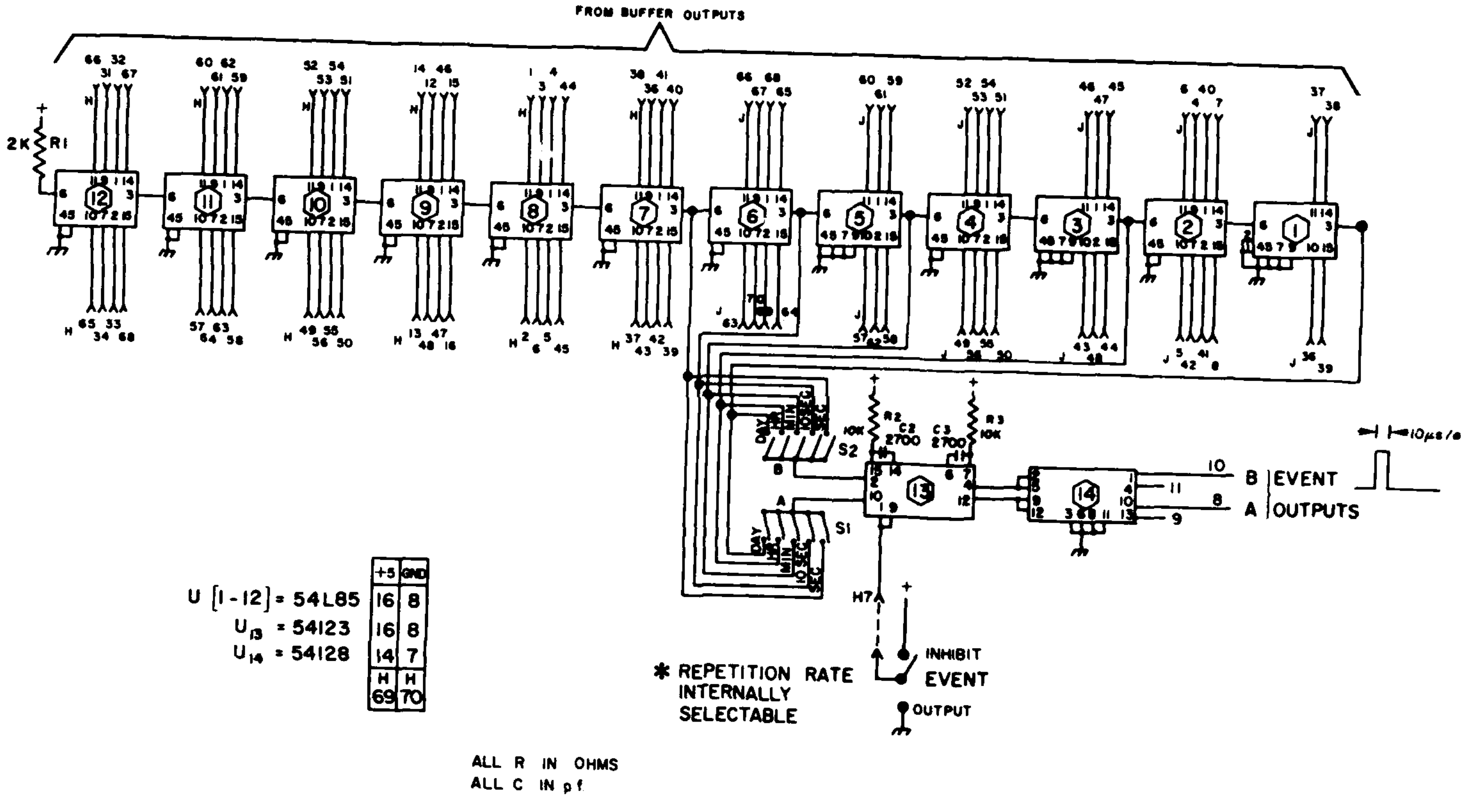
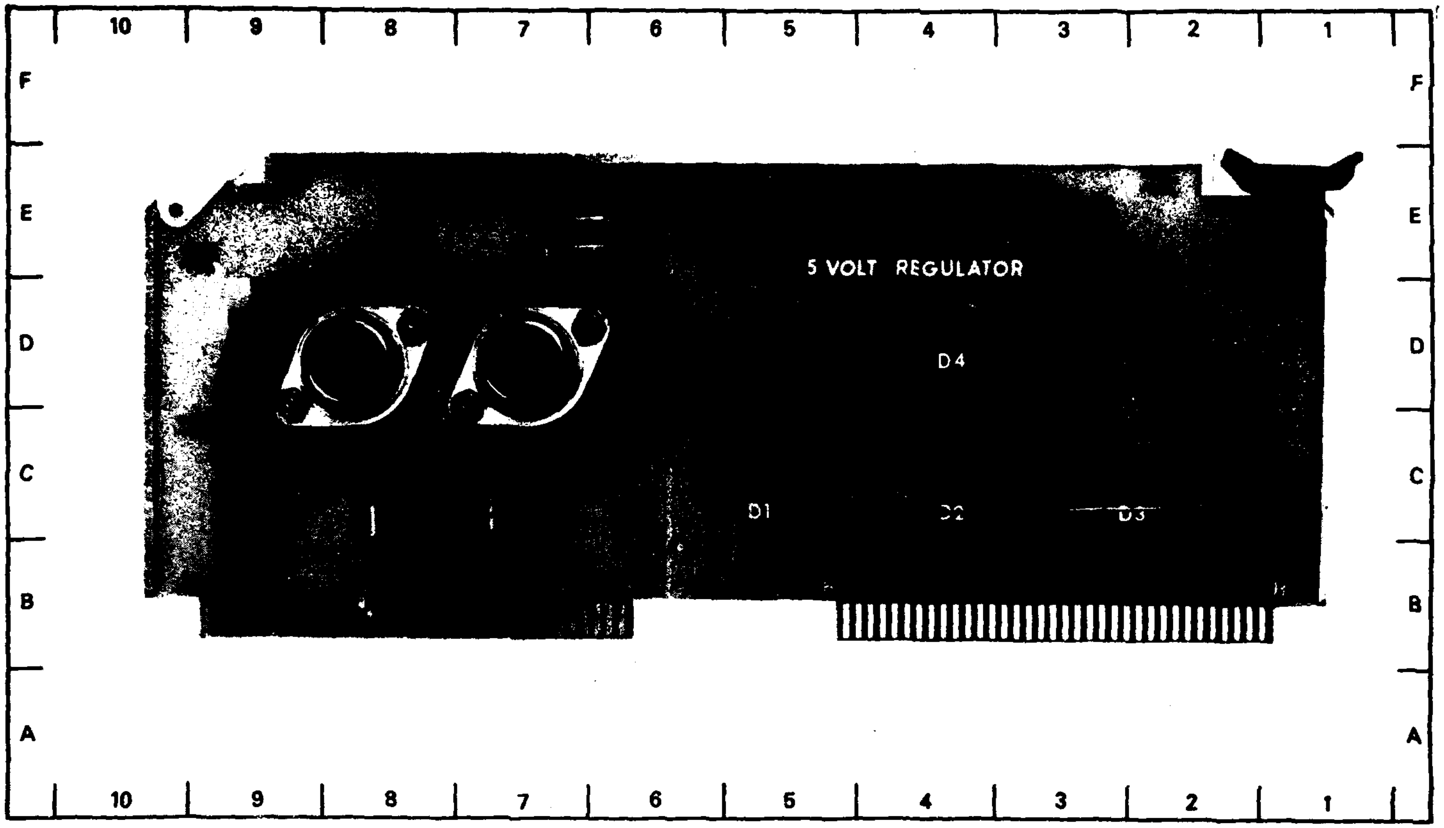


Figure 6-4B—Schematic of Time of Event Circuit (see drawings)



Reference Designation	Location	Reference Designation	Location	Reference Designation	Location
A5C1	E7	A5D1	B5	A5U1	C9
A5C2	E7	A5D2	B4	A5U2	C7
A5C3	B8	A5D3	B2		
A5C4	B7	A5D4	D4		

Figure 6-5A—Parts Location Index, 5 Volt Regulator Board Assembly A5

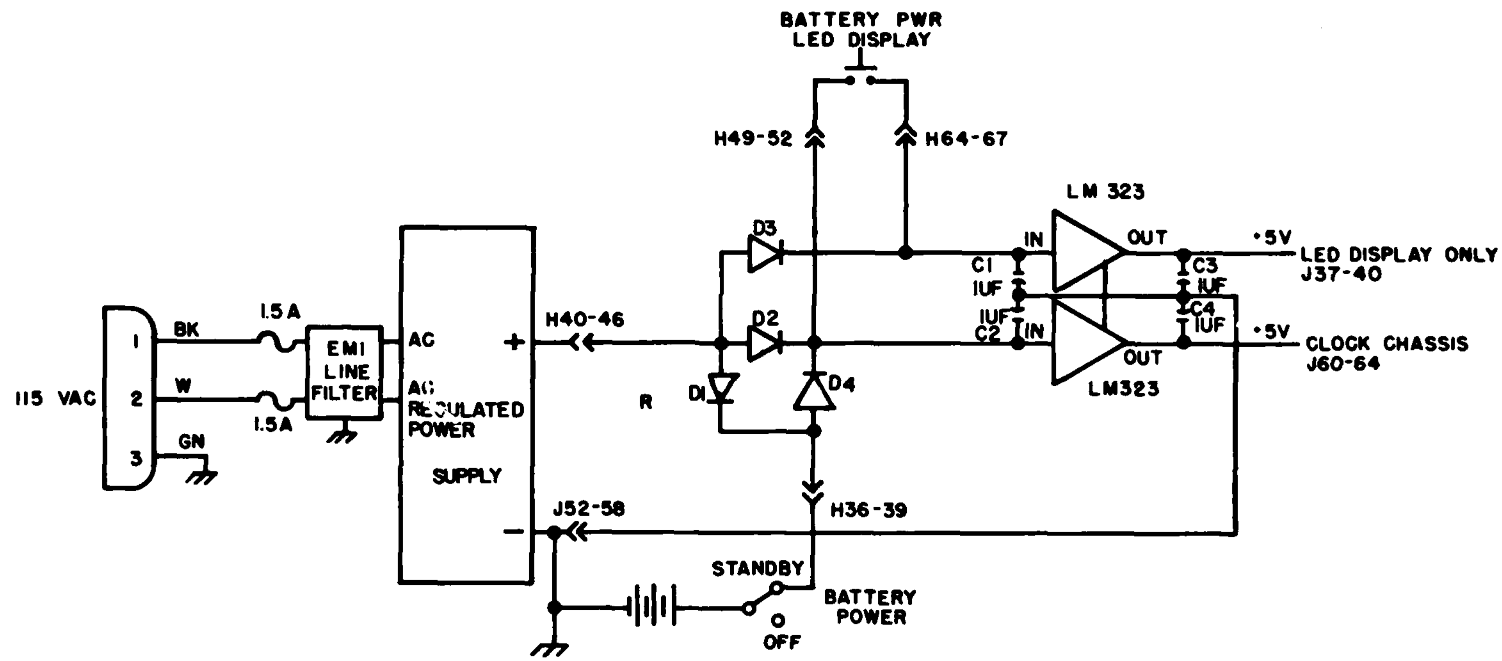


Figure 6-5B—Schematic of 5 Volt Regulator Board (see drawings)

CHAPTER 7

PARTS LIST

7-1 Parts List for the Digital Processing Clock

Tables 7-1 to 7-8 give the parts for the Digital Processing Clock, it assemblies, and its subassemblies.

TABLE 7-1

DIGITAL PROCESSING CLOCK, NRL 184-1, PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
NRL 184-1-A		Chassis-sides, top, bottom rails, and ears, Buckeye Stamping Co. DSC 13.3 by 43.2 by 50.8 cm (5 1/4 by 17 by 20 in), IR 5954-76 IR 17641-76	1-0
NRL 184-1-AA		Front Panel, 0.32 cm (1/8 in) 60-61 aluminum, NRL	1-0
AA1		Thumbwheel Switches, 4.763 cm (1.875 in) High 5.38 cm ((2.12 in) Bead Height) X 1.270 cm (0.500 in) wide, 0.597 cm (0.235 in) white character Height, Front mounting, 10 position Binary Coded Decimal (1-2-4-8) plus compliment, matte black, solder terminations, Digitran series 1300: one Type 13010 with stops to permit dial to read 0,1,2,3 only one Type 13010 with stops to permit dial to read 0,1,2 only two Type 13010 with stops to permit dial to read 0,1,2,3,4,5,6 only eleven Type 13010 with no stops four spacer, 1.27 cm (1/2 in) wide series 13000	1-0

TABLE 7-1

DIGITAL PROCESSING CLOCK, NRL 184-1, PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
		one spacer, 1.27 cm (1/2 in) wide marked with a white decimal point series 13000	
		one spacer, 0.64 cm (1/4in) wide series 13000	
		one pair End piece mounting brackets series 13000	
		Set of Stacks for Series 13000 for 20 station switch assembly	
AA2		Bezel Assembly for use with Dual In Line packaged (DIP) solid state alpha-numeric displays to accept multiple plug in DIP displays, wire wrap term-inations, red filter, 8 position, Industrial Electronic Engineers, Inc. Opto Components Div., IEE type 1750-08R	1-0
AA2A		3 position Bezel Assemply, otherwise same as above, IEE type 1750-03R	1-0
AA3, AA4		BNC connector for 1 PPS and EXT. SYNC, Bendix No. 4890-1	1-0
AA5 through AA7		Pushbutton microswitch for Arm, LED Display and LED test, Micro-switch, Freeport, Ill., Part No. 1 PB5	1-0
AA8 through AA14		Toggle Switch for Battery Standby/off, Event Output/Inhibit, Sync 1PPs/clock and Int/EXT, UND. Lab Inc., 5A-125Vac L117, Micro Switch Part No. ITW1-3 MS 277 16-23	1-0
AA12 through AA14		Line fuse holders, BUSS 20A, 90-250V, FHL 17G1	1-0
AA15 through AA17		Line fuses, one spare, 1.5A Slow Blow	2-2
NRL 184-1-AB		Back Panel, 0.32 (1/8 in), 60-61 aluminum, NRL	2-2

TABLE 7-1

DIGITAL PROCESSING CLOCK, NRL 184-1, PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
AB1		Time Code Out Connector, Cannon Connector SK-24-31SL, 24 pin multi-contact connector	2-2
AB2		Power Connector 115 Vac, Cannon 3 prong connector WK-C3-32SL	2-2
AB3 through AB14		BNC, type D, NRL Supply No. 5935-00-835-0510 connector, receptacle M390 12/21-0001, 6 in lower row used, 6 in upper row spares	2-2
AB15		Power cord and connector, plug electrical type UP221M, NRL Supply No. 5935-00-931-7490	
AB16		Cable connector for time code cable, mates with time code out connector on back of clock, Cannon type SK 24-22C3/4	2-2
NRL 184-1-B1		Power Module, AC-DC, 105-125 VAC 47-420 Hz Input with built-in over-voltage and short circuit protections, Regulated ±0.5% + 1 mv line and load, ripple less than 250 microwatts, adjustable output 0 to 30 dc, 6.6 to 3.4 amps @ 45°C, operation to +71°C with 30% derated output, size 8.096 cm (3-3/16 in) H by 12.54 cm (4 15/16 in) W by 23.81 cm (9-3/8 in) long, Power Mate Model UNI-30D, Power Mate Corp., Hackensack, N.J.	4-1
NRL 184-1-B1A		Power Module Bracket, NRL	4-1
NRL 184-1-B2		Battery, Rechargeable, Sealed, Gelled Electrolyte, 6 V, 4.5 A. hr. at 20-hr. rate, size 15.11 cm (5.95 in) long by 3.404 cm (1.34 in) wide by 10.19 cm (4.01 in) high, 1.04 kg (2.3 lb)., Globe Gell-Cell, Part No. 645-1, Globe Battery Div. of Globe Union, Milwaukee, Wisconsin	4-1

TABLE 7-1

DIGITAL PROCESSING CLOCK, NRL 184-1, PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
B2A		Battery 2 V, 8 A. hr. Globe Gell Cell Part No. GC280, 10.19 cm (4.01 in) by 5.08 cm (2 in) by 4.83 cm (1.9 in)	4-1
B3		Battery bracket, NRL	4-1
NRL 184-1-B4		Line Filter Cornell NF 10431-12 meets MIL-I-16910 2×3.9 A, 125/280 ac at 60 Hz, insertion loss 10 db at 150 kHz, 34 db at 600 kHz, 46 db at 1 MHz, 38 db at 10 MHz	4-1
NRL 184-1-B5		Card File, 13 positions for 24.77 cm by 11.43 cm by 0.157 cm (9.75 in by 4.5 in by 0.062 in) thick cards, without connectors, Cambion Part No. 706-9024-02-00-00	4-1
B5 (1) through B5 (14)		Connector, card edge, 0.25 cm (0.1 in) contact spacing, for 0.159 cm (1/16 in) board thickness 35 positions, double readout, 70 contacts solder lug terminations, Cambion Part No. 706-7029-01-00-00	4-2
NRL 184-1-B6		Power and Ground Bus strip, Cambion Part No. 706-1050-01	4-2
NRL 184-1-B7		Slides, Chassis, Non-Rotating Type Cabinet Sec. 55.88 cm (22 in) NRL Supply No. 5999-S03-0303	4-1

TABLE 7-2

CLOCK TIME BASE CIRCUIT, NRL 184-1-A1A, (CARD SUBASSEMBLY A1A) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A1A		Clock Time Base NRL 184-1-A1A Includes internal temperature compensated crystal oscillator (TCXO) with 1 MHz output; detects and shapes the 1 MHz signal coming from the internal TCXO or external source and applies it to the 1A2 assembly	6-1A
A1AC8		Capacitor, Fixed, Mylar 470 pf, Mil-C-5D Type CM06FD471J03	
A1AC9		Capacitor, Fixed, Mylar 100 pf, Mil-C-5D Type CM04FD101J03	
A1AC10 and A1AC11		Capacitor, Coupling, ceramic molded monolythic, radial leads, 0.01 μf (±10%), 200 WVDC, Reliability Level "S" (0.0001%) Mil Part No. 1M39014/02-1338	
A1ACR1		Diode, 1N4149	
A1AR7* and A1AR9	*A1AR7 has been removed	Resistor, 1.0 kΩ (±5%), 1/4 W	
A1AR11 and A1AR14		Resistor, 1.0 kΩ (±5%), 1/4 W	
A1AR8		Resistor, 6.8 kΩ (±5%), 1/4 W	
A1AR10		Resistor, 2.0 kΩ (±5%), 1/4 W	
A1AR12 and A1AR13		Resistor, 4.7 kΩ (±5%), 1/4 W	
A1AU7		Integrated Circuit, Dual 4 Input Positive NAND Schmitt Trigger, ceramic 14 lead DIP, −55°C to +125°C operating temperature range, Industrial type SN5413J, Federal Stack No. 5962-00-001-6011	

TABLE 7-2

CLOCK TIME BASE CIRCUIT, NRL 184-1-A1A,
(CARD SUBASSEMBLY A1A) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A1AU8		Integrated Circuit, Monostable Multivibrator, Low Power TTL, ceramic 14 lead DIP, -55°C to ±125°C operating temperature range, Industrial type SN54L121J	6-1A
A1AU9		Integrated Circuit, Dual 2 Wide 2-Input AND-OR-Invert Gates, Low Power TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54L51J	
A1AU10		Integrated Circuit, Hex Inverter, Low Power TTL, ceramic 14 lead DIP, -55°C to 125°C operating temperature range, MIL-M35510 Reliability Level Class B, Tin plated leads, Industrial type SN54L04J, Mil Part No. M38510/02005 BCC, Federal Stock No. 5962-00-187-9689, National Semiconductor 7424	
A1AY1		TCXO, 1 MHz output frequency, output drive compatible with TTL load, 5 Vdc power requirement, output stability, $\pm 5 \times 10^{-7}$ over temperature range of 0°C to 70°C, aging stability better than 1×10^{-8} per day and 1×10^{-6} per year, Frequency adjustment to permit recalibration for a 3-year period (minimum), sealed construction for printed circuit board mounting, Vectron Model C0-252 AK, Vectron Laboratories, Inc., Norwalk, Conn. Attaching hardware: Card ejectors (dark red) Scanbe #S200, Los Angeles Calif.	

TABLE 7-3

DISPLAY CIRCUIT, NRL 184 1-A1B, (CARD SUBASSEMBLY A1B) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A1B		Display Circuit, NRL 184-1-A1B Contains indicator and control logic, shapes output pulses, contains output drivers for display and 50 Ω line drivers for variable pulse outputs (1PPs to 1 PP Day)	6-1A
A1BC1 and A1BC3		Capacitor, Fixed, Mylar 2700 pf, Mil-C-5D, Type CM06FD272J03	
A1BC2 and A1BC7		Capacitor, Decoupling, ceramic molded monolythic, radial leads, 0.01 mf ±10%, 200 WVDC, Reliability Level "S" (0.001%), Mil Part No. M39014/02-1338	
A1BC4 and A1BC6		Capacitor, Fixed Mylar 240 pf, Mil-C-5D, Type CM04FD241J03	
A1BC5		Capacitor, tantalum, hermetically sealed, 25 mf ±20%, 8 WVDC, 9.2 volts surge @ 85°C, Mil-C-39006/09-6461 (0.1%/1000 hours failure rate, Mil Equivalent of GE Part No. 69F4115G 135G7)	
A1BR1 and A1BR3		Resistor, 10.0 kΩ ±5%, 1/4 W	
A1BR4 and A1BR5		Resistor, 10.0 kΩ ±5%, 1/4 W	
A1BR2		Resistor, 1.0 kΩ ±5%, 1/4 W	
A1BR6		Resistor, 15.0 kΩ ±5%, 1/4 W	
A1BU1 and A1BU4		Integrated Circuit, Dual Retriggerable Monostable Multivibrator with Clear, Low Power TTL, ceramic 16 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54L123J	
A1BU2		Integrated Circuit, Line Driver, TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54128J	

TABLE 7-3

DISPLAY CIRCUIT, NRL 184 1-A1B, (CARD SUBASSEMBLY A1B)
PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A1BU3		Integrated Circuit, Monostable Multivibrator, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, TTL, MIL-M-38510, Gold plated leads, Reliability Level Class B, Industrial type SN54121J, Mil Part No. M38510/01201BCC, Federal Stock No. 5962-00-007-4076	
A1BU5		Integrated Circuit, Monostable Multivibrator, Low Power TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54L121J	
A1BU6		Integrated Circuit, Hex Inverter, TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Mil-M-38510 Reliability Level Class B, Industrial Type SN5404J, Mil Part No. M38510/00105BCC, Federal Stock No. 5962-00-007-2036 National Semiconductor 7419	

TABLE 7-4

1 MHz TO 1 PPS COUNTDOWN AND SYNC CIRCUIT, NRL 184 1-A2
(CARD ASSEMBLY 2) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A2		1 MHz to 1 PPS Countdown and Sync Circuit, NRL 184-1A2: divides down 1 MHz to 1 PPS and contains synchronization logic	6-2A
A2C1		Capacitor, Fixed, Mylar 150 pfd, Mil-C-5D Type CM04FD151J03	

TABLE 7-4

1MHz TO 1 PPS COUNTDOWN AND SYNC CIRCUIT, NRL 184 1-A2
(CARD ASSEMBLY 2) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A2C2		Capacitor, Fixed, Mylar 120 pf, Mil-C-5D Type CM04FD121J03	
A2C3 through A2C6		Capacitor, Fixed 0.01 mf, 100 V	
A2R1		Resistor, 200 Ω ±5%, 1/4 W	
A2R2		Resistor, 4.7 kΩ ±5%, 1/4 W	
A2R3 through A2R10		Resistor, 1.0 kΩ ±5%, 1/4 W; pull up	
A2U1		Integrated Circuit, Hex Inverter, TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Mil-M-38510 Reliability Level Class B, Industrial type SN5404J, Mil Part No. M38510/00105BCC	
A2U2		Integrated Circuit, Monostable Multivibrator, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, TTL, MIL-M-38510, Gold plated leads, Reliability Level Class B, Industrial type SN54121J, Mil Part No. M38510/01201BCC, Federal Stock No. 5962-00-007-4076	
A2U3		Integrated Circuit, Dual J-K Flip Flop with Clear, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Low power TTL, MIL-M-38510, Gold plated leads Reliability Level Class B, Industrial Type SN54L73J	
A2U4 and A2U5		Integrated Circuit, Quadruple 2 Input Positive NAND Gates, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, TTL, MIL-M-38510, Gold plated leads, Reliability Level Class B, Industrial type SN5400J; Mil Part No. M38510/00104BCC Federal Stock No. 5962-00-762-0645	

TABLE 7-4

1MHz TO 1 PPS COUNTDOWN AND SYNC CIRCUIT, NRL 184 1-A2 (CARD ASSEMBLY 2) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A2U6, A2U14, A2U15, A2U16, and A2U17		Integrated Circuit, Hex Inverter Buffer/Driver with Open Collector High Voltage Output, ceramic 14 lead DIP, TTL, -55°C to W125°C operating temperature range, Industrial type SN5417J	6-2A
A2U7, A2U19, and A2U21		Resistor Network— 13 resistors each 470 Ω ±2%, 1/8 Watt at 40°C resistors packaged in 14 lead DIP, one common lead, manufactured by Allen Bradley, Part No. 34A4714	
A2U8, A2U9, A2U10, A2U11, A2U12 and A2U13		Integrated Circuit, Synchronous 4 Bit up/down Decade Counter, Low Power TTL, ceramic 16 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54L192J, manufactured by National Semiconductor, Part No. DM75160J	
A2U18, A2U20, A2U22		Resistor Network—13 resistors each 1 kΩ (±2%), 1/8 W resistors packaged in 14 lead DIP, one common lead, manufactured by Allen Bradley, Part No. 34A1024	
		Attaching Hardware: 2 Card Ejectors 0.952 cm (0.375 in) wide for 0.159 cm (1/15 in) card thickness (red), Scanbe No. S-200, Los Angeles, Calif.	

TABLE 7-5

DAY HOUR MINUTE SECOND COUNTER NRL 184-1A3 (CARD 3) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A3		Day Hour Minute Second Counter NRL 184 1A3; generates buffered time of day information to remote readouts	6-3A
A3C1, A3C4, A3C5 and A3C6		Capacitor, Fixed, disk 0.01 mf, 100 V	
A3C2 and A3C3		Capacitor, Fixed, tantalum, hermetically sealed, 25 mf ±20%, 8 WVDC, 9.2 V surge @ 85°C, Mil-C-39006109J GE part #69F4115	
A3C7-A3C9		*individually selected, Capacitor, mylar, 0-300 pf	
A3R1—A3R39		Resistor, 1.0 KΩ (±5%) 1/4 W	
A3S1		Switch, Leap Year, Toggle, Right Angle Printed Circuit Mounting, SPDT, On-None-On, 5 A., 28 Vdc or 115 Vac, C&K Part No. 7101A	
A3U1 through A3U9		Integrated Circuit, Synchronous 4 Bit Up/Down Decade Counter, Low Power TTL, ceramic 16 lead DIP, -55°C to +125°C operating temperature range, Industrial type SN54L192J, manufactured National Semiconductor, Part No. DM75L60J	
A3U10, A3U12, A3U14, A3U17, and A3U18		Integrated Circuit, Hex Inverter Buffer/ Driver with Open Collector High Voltage Output, ceramic 14 lead DIP, TTL, -55°C to +125°C operating temperature range, Industrial type SN5417J	

TABLE 7-5

DAY HOUR MINUTE SECOND COUNTER NRL 184-1A3
(CARD 3) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A3U11, A3U13, and A3U15		Integrated Circuit, Quadruple 2 Input Positive NAND Gate, Low Power TTL, 14 lead ceramic DIP, -55°C to +125°C operating temperature range, Tin plated Level Class B, Industrial Type SN54L00J, Mil Part No. M38510 02004BCB	
A3U16		Integrated Circuit, Quadruple 2-Input Positive NOR Gates, TTL Low Power, ceramic 14 lead DIP, -55°C to +125°C operating temperature range, Tin plated leads MIL-M-38510, Reliability Level Class B, Industrial type SN54L02J	
A3U19, A3U20, and A3U22		Resistor Network—13 resistors each 470 Ω (±2%), 1/8 W at 40°C resistors packaged in 14 lead DIP, one common lead, manufactured by Allen Bradley, Part No. 34A4714	
A3U21		Integrated Circuit, 8-Input Positive NAND Gate, Low Power TTL, ceramic 14 lead DIP, -55°C to +125°C operating temperature range Industrial Type SN54L30J, Mil Part No. M38510/02001BCB	
		Attaching hardware: 2 card ejectors (orange) Scanbe S200 Los Angeles, Calif.	

TABLE 7-6

TIME OF EVENT CIRCUIT (NRL 184-1A4) (CARD 4) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A4		Time of Event Circuit, NRL 184-1-A4 generates time of event pulse or pulses	6-4A
A4C1, A4C2, A4C3, and A4C7		Capacitor, Fixed, disk, 0.01 mf	
A4C4		Capacitor, Fixed, tantalum, hermetically sealed, 25 mf (±20%), 8 WVDC, 9.2 V surge at 85°C, MIL-C-39006/09-6461 (0.1%/1000 h failure rate, MIL Equivalent of GE Pt. No. 69F4115G 135G7)	
A4C5, A4C6		Capacitor, Fixed, mylar 2700 pf, MIL-C-SD type CM06FD272J03	
A4R1		Resistor, 2.0K Ω (±5%) 1/4 W	
A4R2, A4R3		Resistor, 10.0K Ω (±5%) 1/4 W	
A4S1, A4S2		Switch, DIP packaged Rocker Switches, 8 single-pole-single-throw switches per pkg., 5V 100 mA contact rating, manufactured by AMP, Inc., Part No. 435166-5 7524	
A4U1 thru A4U12		Integrated Circuit, 4 Bit Magnitude Comparator, ceramic 16 lead DIP, Low power TTL, - 55°C to +125°C operating temperature range, Industrial type SN54L85J, Federal Stock No. 5962-00-481-9361	
A4U13		Integrated Circuit, Dual Retriggerable Monostable Multivibrator with Clear, TTL, 16 lead ceramic DIP, - 55°C to +125°C operating temperature range, MIL-M-38510, Gold plate leads, Reliability Level Class B, Industrial type SN54123J, Mil Part No. M38510/01203BED, Federal Stock No. 5962-00-173-3911	

TABLE 7-6

TIME OF EVENT CIRCUIT (NRL 184-1A4) (CARD 4) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
A4U14		Integrated Circuit, Line Driver, TTL, ceramic 14 lead DIP, - 55°C to +125°C operating temperatures range, 75 Ω, Industrial type SN54128J Attaching Hardware: 2 Card Ejectors (green) Scanbe S200 Los Angeles, Calif.	

TABLE 7-7

5 VOLT REGULATOR (NRL 184-1-A5) (CARD 5) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A5		5 Volt Regulator Board NRL 184-1-A5 provides regulated 5 V power to run integrated circuits (ICs) and readouts in Digital Processing Clock.	6-5A
A5C1, A5C2, A5C3, and A5C4		Capacitor, Fixed, electrolytic, tantalum, 1.0 mf (±10%), 35 Vdc	
A5D1, A5D2, A5D3, and A5D4		Diode, 1N1614, GE, Part No. 7426F	
A5U1 and A5U2		Integrated Circuit, Voltage regulator, 323 3A, National Semiconductor part No. 514 LM323K, 0°C to 70°C operating temperature range Attaching Hardware: Heat sink for two voltage regulators Four 10-32 lockwashers and nuts for diodes Attaching Hardware: Card Ejectors (black) Scanbe S200 Los Angeles, Calif.	

TABLE 7-8

READOUT INTERFACE BOARD NRL 184-1-A6 (A6) AND SHIELD CARD NRL 184-1-A7 (A7) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
A6		70 pin Readout interface plug-in board	4-1
A7		Shield card, 0.159 cm (1/16 in) unetched, micarta board, attaching hardware: 2 card ejectors (yellow), Scanbe S200, Los Angeles, Calif.	4-1

7-2 Parts List for the Remote Display Unit

Table 7-9 is a parts list for the Remote Display Unit.

TABLE 7-9

REMOTE DISPLAY UNIT (NRL 184-2) PARTS LIST

Reference Designation	Notes	Name and Description	Figure Number (Item)
NRL 184-2		Remote Display Unit—gives readout of 20 line time code from clock of hours, minutes and seconds	3-3
2-A1		Power Module, ac-dc; 105 to 125 Vac, 50-420 Hz input, +5V dc 2 AMP output ±0.05% Line Regulation, ±0.20% load regulation, 1 mV maximum ripple, operating temperature range 0° to 71°C without derating, barrier strip connections, chassis mounting with 4 threaded inserts on side opposite terminal board, 6.35 cm by 8.89 cm by 6.03 cm (2-1/2 in) by 3-1/2 in by 2-3/8 in high maximum. Semiconductor Circuits Model CM 5S2000	3-4
2-A2		24 Pin Wire Wrap socket, Scanbe Stock No. ME-2B-24-W-G-B-10	

TABLE 7-9

REMOTE DISPLAY UNIT (NRL 184-2) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
2-A3		Switch, Push Button, moistureproof, push-push action, DPDT Single Break, Red Push Button, Cutler Hammer part No. J313 PB6R, Federal Stock No. S9E 5930-00-903-8064 MIL-S-8805/36A Type MS17975-6	3-3
2-A4		Bezel Assembly for use with DIP Solid State Alpha Numeric Displays, to accept multiple plug in DIP displays, wire wrap terminations, red filter, Industrial Electronic Engineers Inc. Opto Components Div., IEE type 1750-08R	3-4
2-A5 thru 2-A10		Solid State visible seven segment display, TI type TIL 308, 0.69 cm (0.27 in) character height, capable of displaying characters 0 through 9 with left decimal point, 5 Vdc operation with 250 ma maximum current, integral self-contained latch, decoder and driver circuits, DIP package configuration 0.76 cm (0.3 in) row spacing w/0.25 cm (0.1 in) lead center, 660 nanometer wavelength output, 1200 ncd luminous intensity, TTL compatible, 4 line BCD plus Decimal point input, operating temperature range 0°C to 70°C	
J1		Time Code in Connector on back panel, Cannon connector SK-24-32SL, 24 pin multicontact connector	3-4
J2		Time Code out Connector on back panel, Cannon Connector SK-24-31SL, 24 pin multicontact connector	3-4

TABLE 7-9

REMOTE DISPLAY UNIT (NRL 184-2) PARTS LIST—(Continued)

Reference Designation	Notes	Name and Description	Figure Number (Item)
J3		Power Connector on Back, Cannon 3 prong connector WK-C3-32SL	3-4
2-A11		Fuse holder—Buss NRL Supply No. 133218	
2-A12		Fuse, cartridge, 3/8 A slow blow, Type F02B250V3/8AS DSA900-75-M-GH94	
2-A13 and 2-A14		0.22 mf 200 Vdc, PUP MPY 2P22 capacitor	
2-A15		Chassis—NRL 184-2A	3-4
2-A16		Power cord—connector, Plug Electrical Type UP 221M NRL Supply #5935-00-931-7490	
2-A17		Cable connector, mates with J1, Cannon type SK 24-21C3/4	
2-A18		Cable connector mates with J2, Cannon type SK 24-22C3/4	

7-3 Parts Location Index

A parts location index is supplied for the five plug-in boards of the Digital Processing Clock and is found in Chapter 6 with Figures 6-1A, 6-2A, 6-3A, 6-4A, and 6-5A.

VIII. CHAPTER 8

INSTALLATION

The Digital Processing Clock has slides mounted on the side of the chassis for mounting it in a standard 48 cm (19 in) rack. Connectors are supplied to be installed on 21 line cables to go from the Digital Processing Clock's Time Code Out cannon plug (Fig. 2-2) on the clock's back panel to the J1 cannon connector (Fig. 3-4) on the back panel of the first remote display unit and likewise for the cable to go from the J2 cannon connector (Fig. 3-4) on the back panel of the first remote display unit to the JL cannon connector of the second remote display unit and similarly, for the third and fourth remote display units. In wiring the cannon cable connector SK24-22C 3/4 to the end of cable which plugs into the Time Code Out on the back of the Digital Processing Clock, and the cannon cable connector SK24-21C 3/4 to the other end of the cable, which connects to J1 on the back panel of the remote display unit, be certain the same wire goes to pin 1 of each of the connectors and, likewise, for pins 2 through 21. Pin 21 is ground.

Five power cords are supplied for the Digital Processing Clock and four Remote Display units. Plug into 115 Vac, 60 Hz, single phase source. The Digital Processing Clock will come on when plugged in—see Table 2-1 Turn-On Procedure. Table 2-2 Functional Checkout Procedure, and Table 2-3 Setting Procedure. After clock is installed, checked out and set, connect cable that you have put the connectors on, as has been described, between Digital Processing Clock and the Remote Display Unit. Plug the Remote Display Unit into 115 Vac, 60 Hz, single-phase source. Push red button on front to start display.

When making cables for the clock, be certain they are long enough for the clock to be pulled forward out of the rack on its slides.

If it is necessary to remove the top cover of the Digital Processing Clock such as to change Leap Year Switch on top of the DAY, HOUR, MINUTE, SECOND COUNTER Board in January 1977 or change Time of Event (TOE) switches A and B on TOE Board, follow the following procedure. Pull clock forward on slides; remove screws holding top cover on, which are located at the top of the back panel, and slide cover backward to allow access to switches.

2137 TIME CODE GENERATOR OPERATION

GENERAL

Board A7 of the Digital Processing Clock uses the timing information
The XR3 unmodulated time code,
present in the clock to produce the serial 2137 time code, and a 200 KHz sine wave signal which are available at the back panel on BNC connectors.
The output impedance of XR3 Unmodulated code is 50 Ω
remaining
The output impedance of both signals is approximately 1 kohm.

The board is organized into three general areas, each of which accomplishes a specific function. The first area covering roughly the right half of the board is the digital section where the pulse width modulated serial digital code is produced. Next to this, covering about the next quarter of the board is the 1 KHz sine wave generator and modulator where the digital code is used to amplitude modulate the 1 KHz sine wave. The final quarter on the left hand side of the board contains the 200 KHz generator and output transformer.

DETAILED

Shown in Fig. 1 is the block diagram of the digital portion of the circuit which produces the pulse width modulated serial digital code. The numbers on the left side of the drawing (A4H38) indicated the card (A4) and the pin number (H38) whence this input line receives its signal. The input lines at the top of the diagram, labeled TOD Data Input, are the timing information in hours, minutes, and seconds in BCD format which are to be converted into the serial time code word. The only output from this circuit is the Time Code Output at the right side, which is the serial digital code.

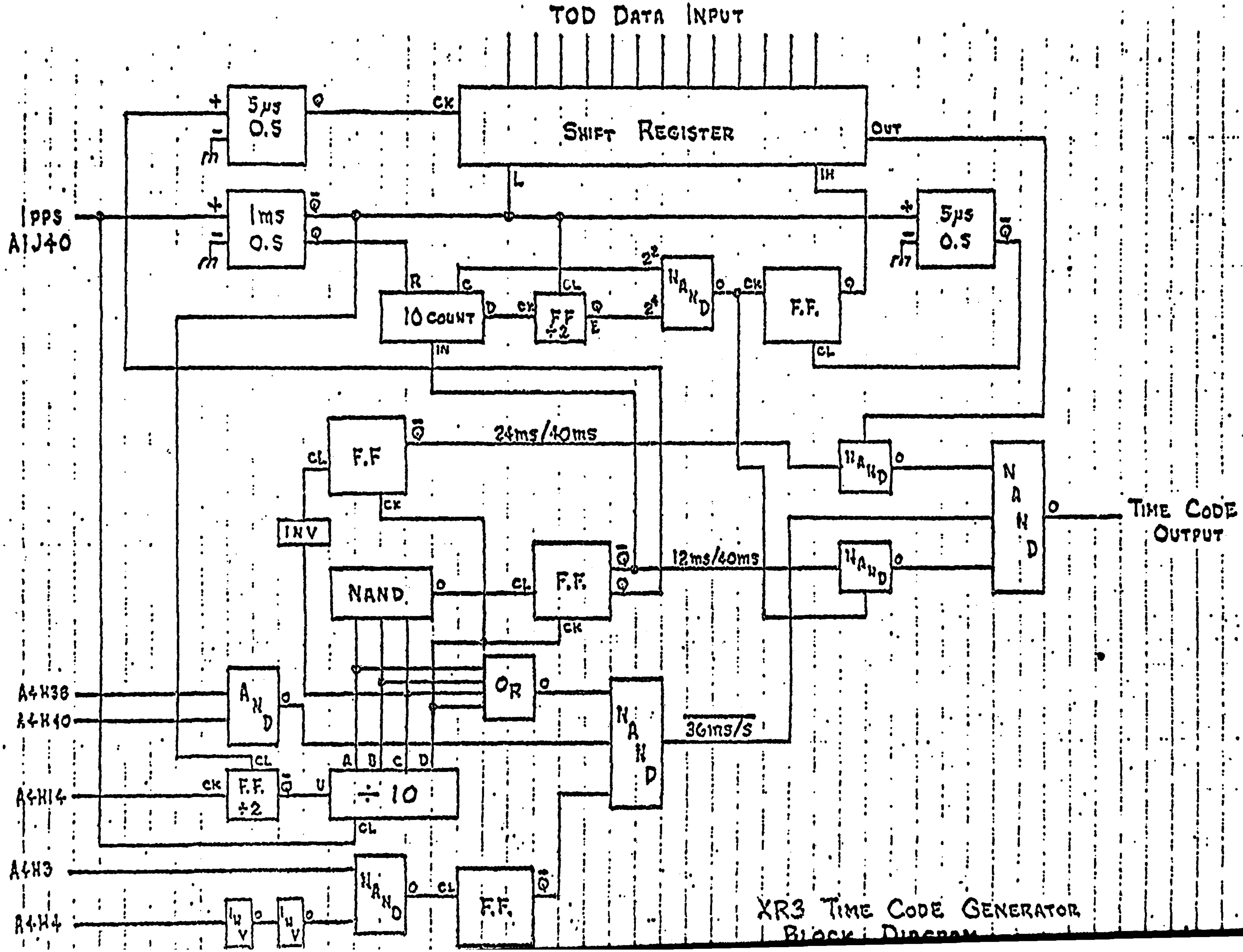
In order to produce the serial time code it is necessary that three distinct signalsbe generated by this circuit. The first is a 12 ms pulse train, recurring every 40 ms, whose falling edge is on time; the second is a 24 ms pulse train, recurring every 40 ms, whose falling edge is also on time; and the third is a 36 ms pulse train, recurring once a second, whose falling edge is again on time. Figure 2 shows the detailed circuit diagram, which is part of Fig. 1, that generated these signals from the inputsprovided. Note that the bar over the labeled output pulse train means that the signal is inverted. Using these signals and the time of day information fed into the shift registers, the circuit diagram of Fig. 3 (also part of Fig. 1) produces serial digital time code. The 1 PPS tick pulse triggers U2 to

generate a 1.2 ms pulse at pin 6 and a negative going pulse at pin 1. This negative going pulse loads the shift register with the parallel time of day information and clears counter U9 while the positive going pulse clears counter U8. At the end of the 1.2 ms pulse one-shot $U10_B$ is triggered which in turn clears flip-flop $U9_B$ enabling the clock input of the shift register. Counters U8 and $U9_A$ are enabled to begin counting input pulses of the 12ms/40ms pulse train. At the same time one-shot $U10_A$ begins sending clocking pulses every 40 ms to the clock input of the shift register. Each clock pulse shifts the data in the shift register one bit to the right and eventually outputs it from pin 9 of U5. When counters U8 and $U9_A$ reach a count of 20 a pulse is sent to clock flip-flop $U9_B$ to its "1" state, thus inhibiting clocking of the shift register. At this time gate $U14_C$ is also inhibited by the counters. The result is that the shift register is clocked precisely 20 times, thus the 20 bits of time of day information have emerged in a serial format from pin 9 of U5. From there it is fed to gate $U14_A$ where it is "ANDed" with the 24ms/40ms pulse train to produce a 24ms pulse every 40ms if the corresponding bit from the shift register is a "1" or no pulse at all in the 40ms interval if the corresponding bit from the shift register was a "0". This signal along with 20 pulses from the 12ms/40ms pulse train and one pulse from the inverted 36ms/sec pulse train are then combined in the 3-input NAND gate $U12_C$, whence the serial digital time code energes at pin 8.

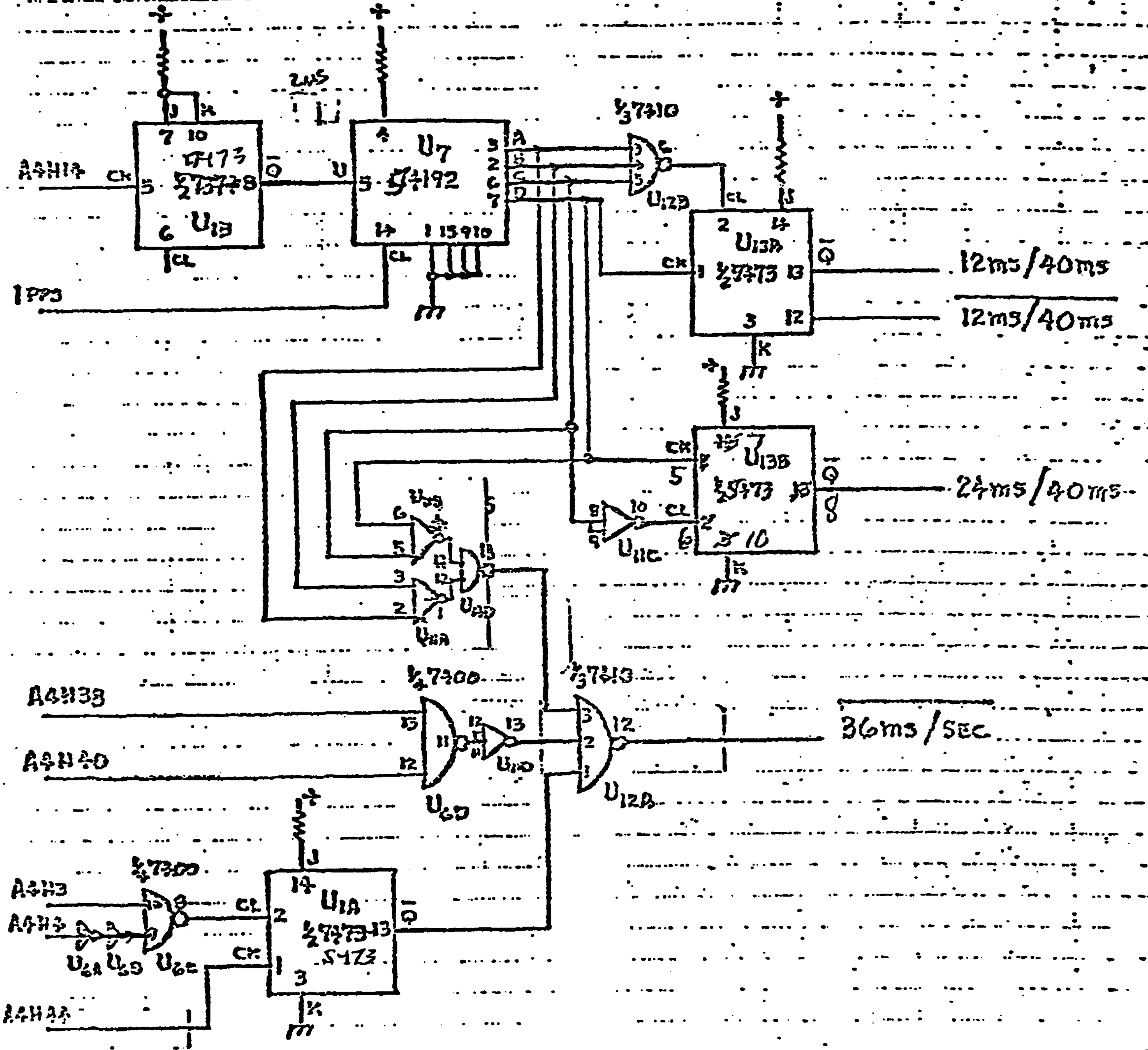
The digital code is then sent to analog switch U16 where it is used to toggle the single-pole double throw switch on and off. Meanwhile a 1 KHz pulse train from A4H51 is fed to U15 where it is filtered to produce a 1 KHz sine wave which is fed to switch U16. The action of U16 causes a modulated 1 KHz sine wave to emerge from pin 5 whose ratio of zero to one level can be controlled over a range from about 2:1 to 6:1 with the pot at the top edge of card. From U16 the signal is fed on to output amplifier U17, whose gain is also adjustable via at pot on the top edge of the card, and from there to the BNC connector on the back panel of the clock.

The final circuit on the card is the 200 KHz sine wave generator, shown in Fig. 5. The 1 MHz square wave from A1H36 is divided by five in U18 and fed to one-shot U19 which restores its 50% duty cycle. Next the signal is filtered by the 200 KHz tuned circuit consisting of L and C and passed on

to the output amplifier Q2, whose gain is adjustable with another pot located along the top edge of the card. From Q2 the signal is passed to emitter follower Q1 which is used to drive the output transformer which steps the voltage up by about 2:1 and sends the signal to the BNC output connector on the back panel of the clock.



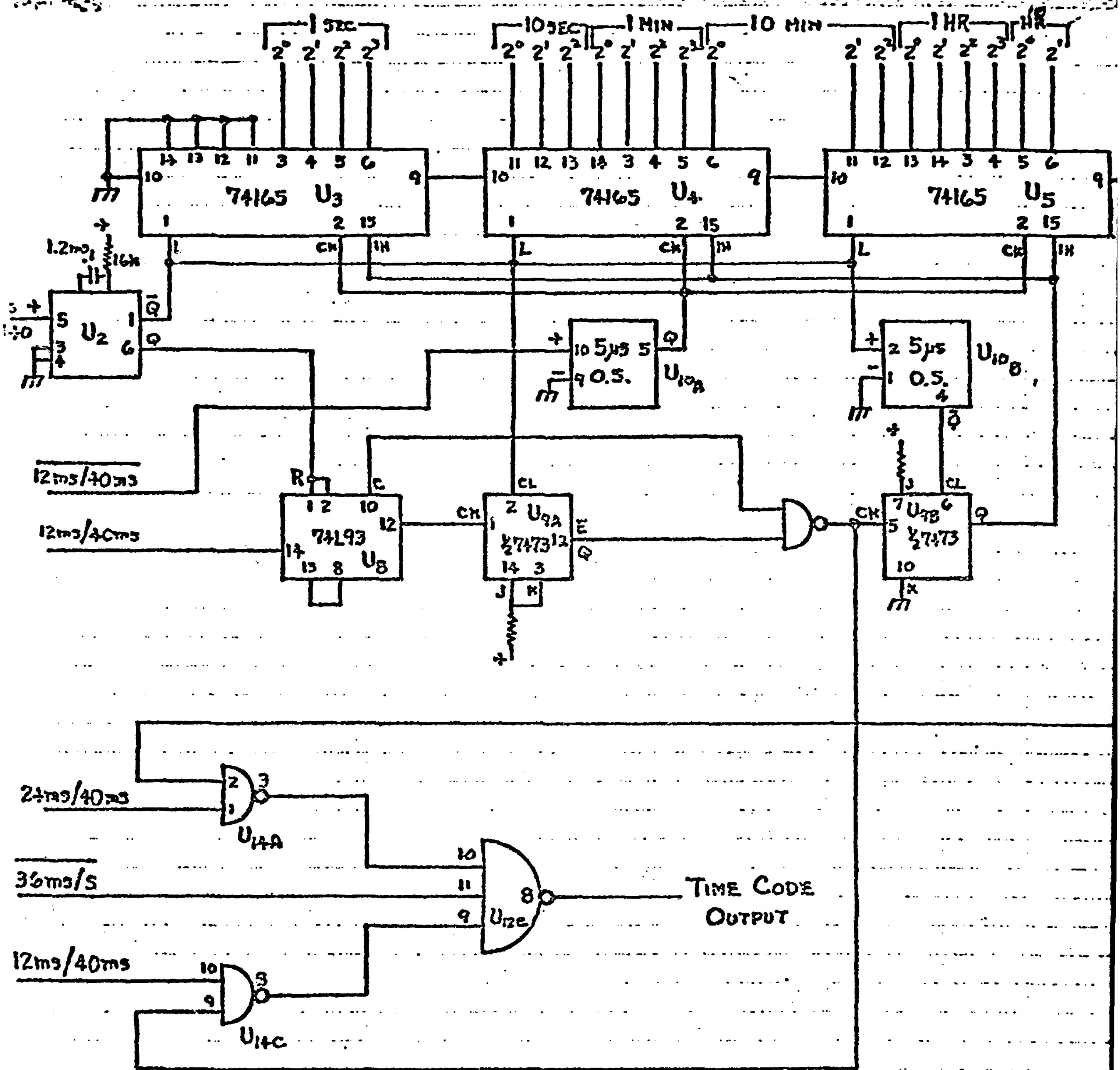
XR3 TIME CODE GENERATOR
Block Diagram



	No	+5	GND
54192	1	16	8
5473	2	4	11
5410	1	14	7
5425	1	14	7
* 5400	1	14	7
54L04	1	14	7

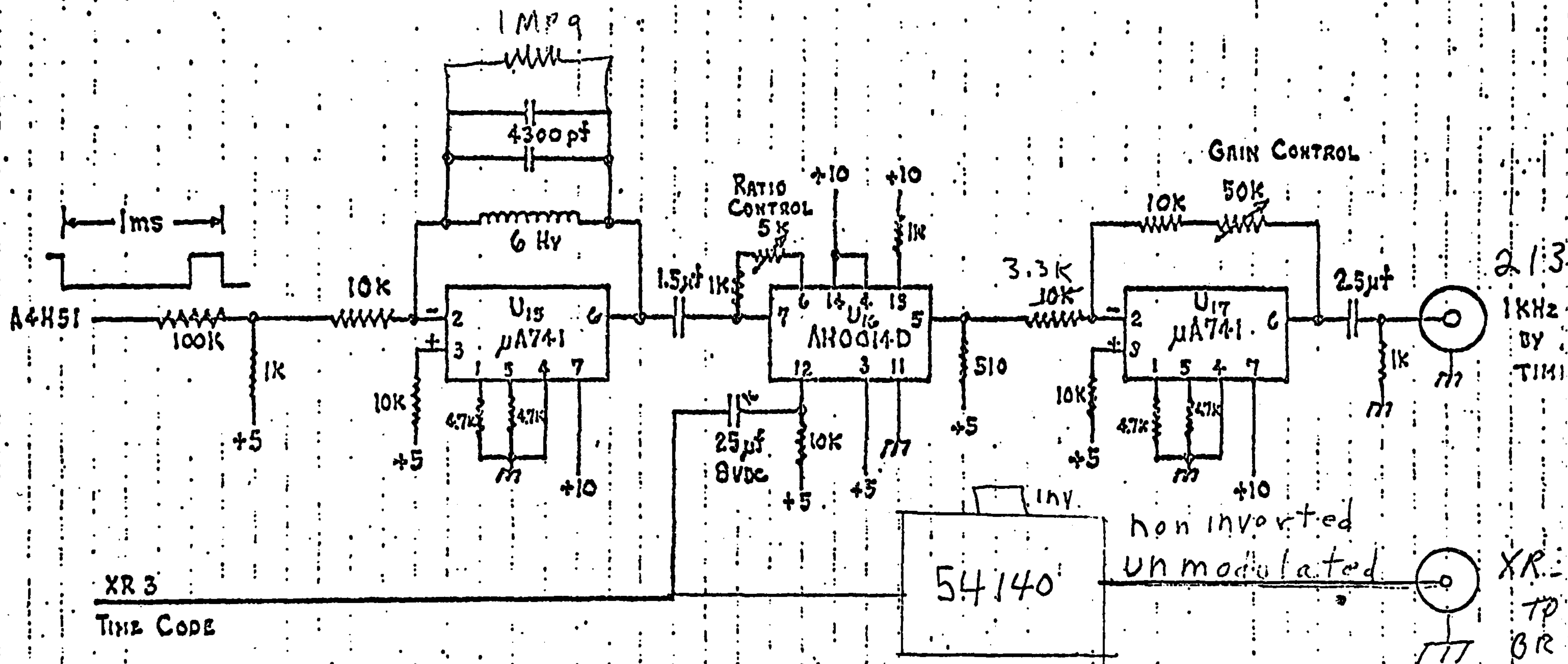
FIG. 2

* OPTIONAL (CAN USE GATES IN '10 AND '25)



XR3 TIME CODE GENERATOR

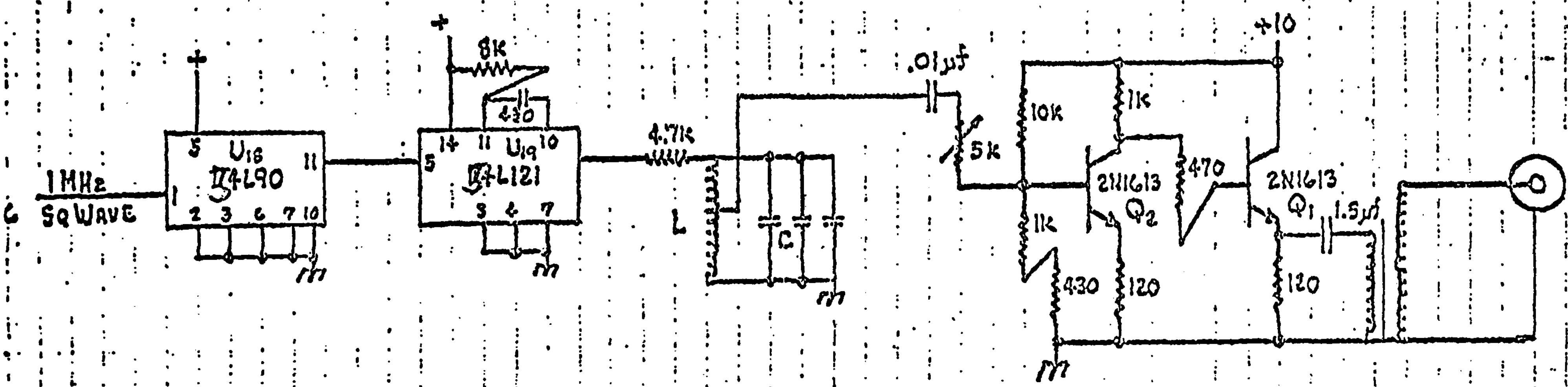
FIG 3



R IN OHMS

1KHz SINE WAVE AND MODULATOR

FIG. 4



L WHITE CORE
160 TURN TAP AT 80T AND 50T

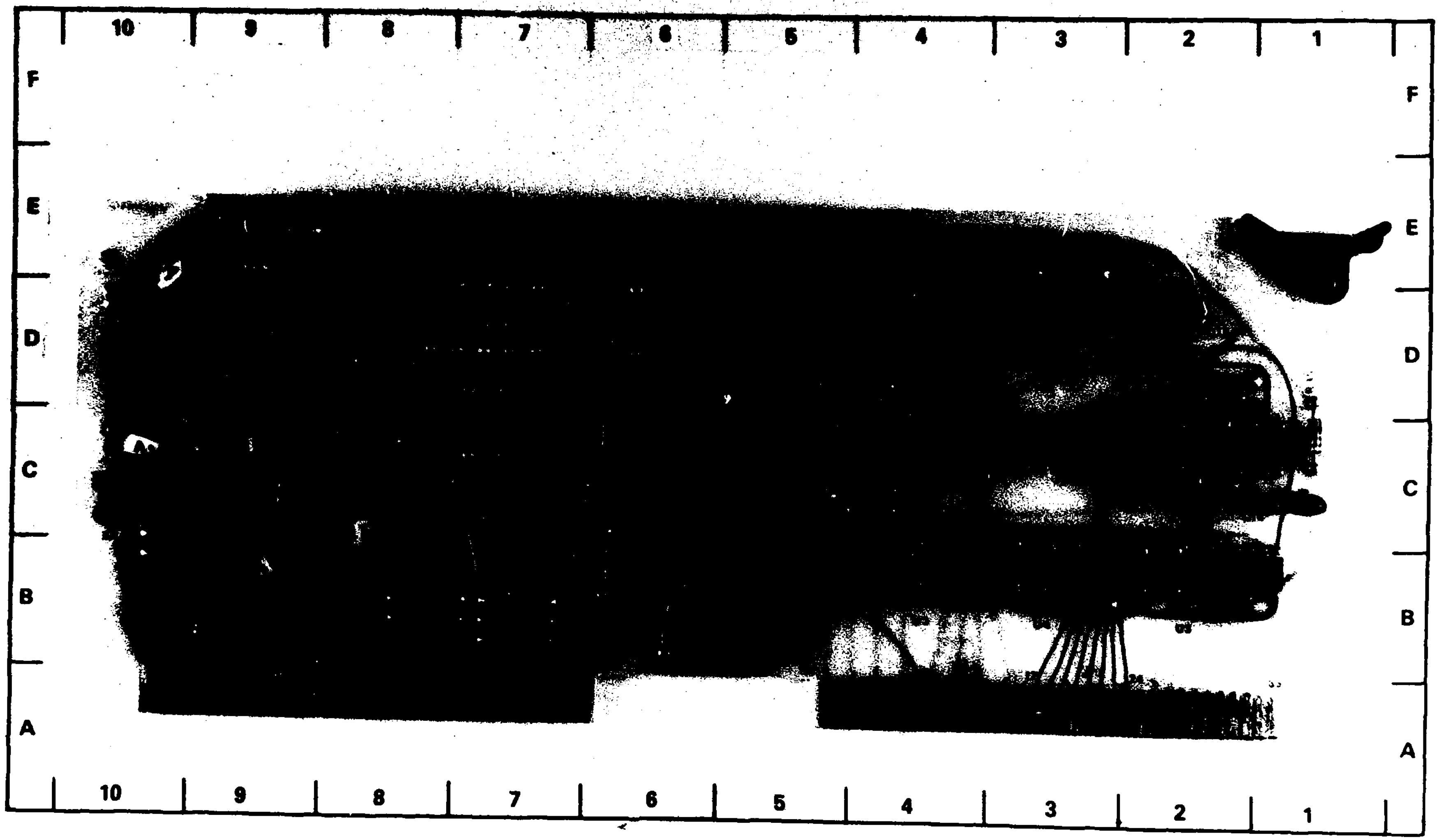
$L = N^2(.0196 \times 10^{-6}) = 0.5\,mh$

$C \doteq 1300$ pf.

R IN OHMS
C IN pf. UNLESS SPECIFIED

200 KHz SINE WAVE GENERATOR

FIG. 5



10 9 8 7 6 5 4 3 2 1
F E D C B A


WARNING!!!

6-8

DTI